

MAX25256

Automotive, 36V H-Bridge Transformer Driver for Isolated Supplies

General Description

The MAX25256 H-bridge transformer driver provides a simple solution for making isolated power supplies up to 10W. The device drives a transformer's primary coil with up to 300mA of current from a wide 8V to 36V direct current (DC) supply. The transformer's secondary-to-primary winding ratio defines the output voltage, allowing selection of virtually any isolated output voltage.

The device features adjustable current limiting, allowing indirect limiting of secondary-side load currents. The current limit of the MAX25256 is set by an external resistor. A $\overline{\text{FAULT}}$ output asserts when the device detects an overtemperature or overcurrent condition. In addition, the device features a low-power mode to reduce the overall supply current to 0.65mA (typ) when the driver is not in use.

The device can be operated using the internal oscillator or driven by an external clock to synchronize multiple MAX25256 devices and precisely set the switching frequency. Internal circuitry guarantees a fixed 50% duty cycle to prevent DC flow through the transformer, regardless of which clock source is used.

The device is available in a small 10-pin (3mm x 3mm) TDFN package and is specified over the -40°C to +125°C automotive temperature range.

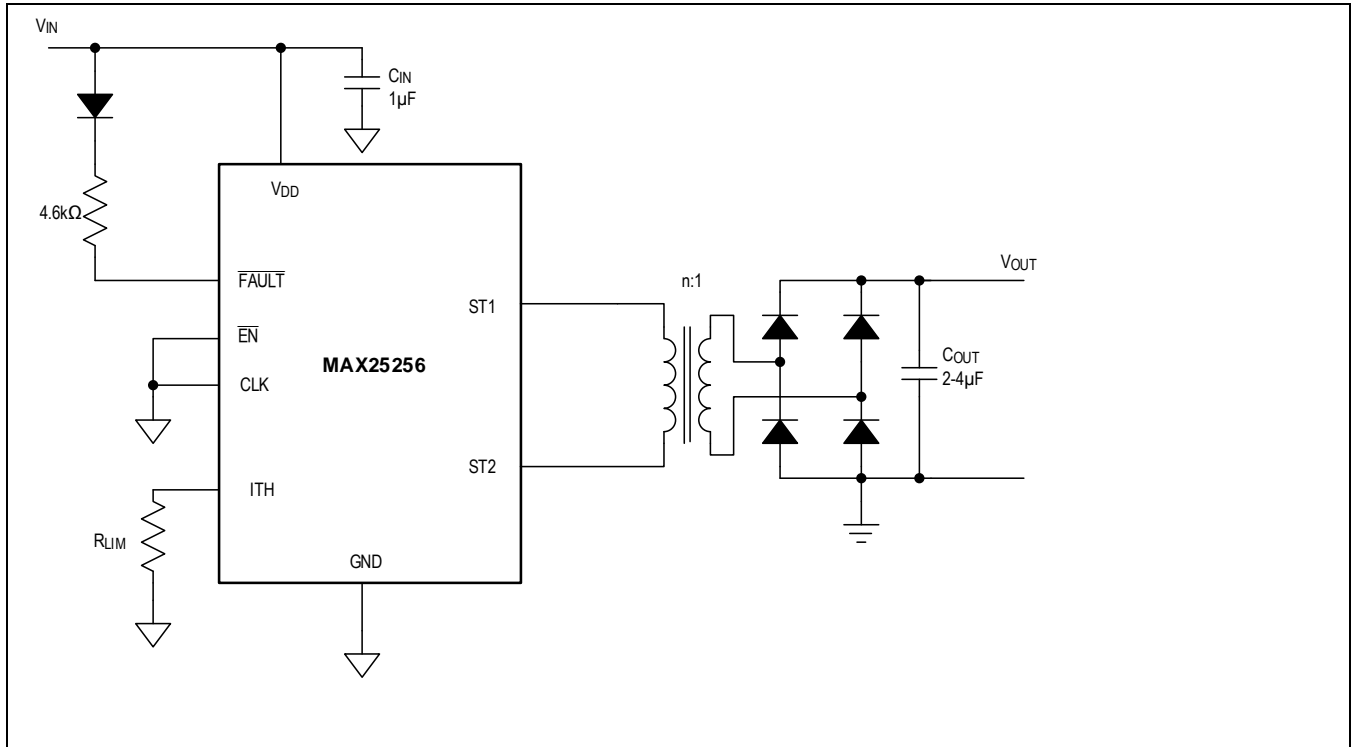
Applications

- Isolated Gate Driver Supplies
- Isolated Supplies for Motor Control
- Dual-Battery Systems
- Isolated Supplies for controller area network (CAN), serial peripheral interface (SPI), I2C, etc.

Benefits and Features

- Simple, Flexible Design
 - 8V to 36V Supply Range
 - Up to 90% Efficiency
 - Provides Up to 10W to the Transformer
 - Undervoltage Lockout (UVLO)
 - 2.5V to 5V Compatible Logic Interface
 - Internal or External Clock Source
 - Adjustable Overcurrent Threshold
- Integrated System Protection
 - Fault Detection and Indication
 - Overcurrent Limiting
 - Overtemperature Protection
- Saves Space on Board
 - Small 10-Pin TDFN Package (3mm x 3mm)
 - AECQ-100 Qualified

Simplified Block Diagram



Absolute Maximum Ratings

V _{DD} , $\overline{\text{FAULT}}$	-0.3V to +40V
ST1, ST2	-0.3V to (V _{DD} + 0.3V)
CLK, I _{TH} , $\overline{\text{EN}}$	-0.3V to +6V
$\overline{\text{FAULT}}$ Continuous Current	±50mA
ST1, ST2 Continuous Current	±850mA
TDFN (Single-Layer Board) (Derate 18.5mW/°C above +70°C)	1481.5mW

Operating Temperature Range	-40°C to +125°C
Operating Junction Temperature (Note 1)	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

10 TDFN-EP

Package Code	T1033+1C
Outline Number	21-0137
Land Pattern Number	90-0003
Thermal Resistance, Single-Layer Board:	

Junction-to-Ambient (θ_{JA})	54°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{DD} = 8V$ to $36V$, $V_{EN} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$ unless otherwise noted, Typical values are at $T_A = +25^\circ C$ (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Voltage Range	V_{DD}	(Note 3)	8		36	V
Supply Current	I_{DD}	$V_{EN} = 0.8V$, $V_{CLK} = 0V$, $R_{LIM} = 1000\Omega$, ST1/ST2 not connected		6	11	mA
Disable Supply Current	I_{DIS}	$V_{EN} = 3.3V$, $V_{CLK} = 0V$		0.7	1.1	mA
Driver Output Resistance	R_{OH}	ST1 = ST2 = high, $I_{ST1, ST2} = +300mA$, $R_{LIM} = 1000\Omega$		1	1.8	Ω
	R_{OL}	ST1 = ST2 = low, $I_{ST1, ST2} = -300mA$, $R_{LIM} = 1000\Omega$		0.6	1.0	
Undervoltage-Lockout Threshold	V_{UVLO}	V_{DD} rising	5.9	6.3	6.9	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVLO_HYST}			300		mV
ST1, ST2 Current Limit	I_{LIM}	$R_{LIM} = 1000\Omega$, $V_{DD} = 24V$	500	650	800	mA
		$R_{LIM} = 3010\Omega$, $V_{DD} = 24V$	165	215	265	
ST1, ST2 Leakage Current	I_{LKG}	$V_{EN} = 3.3V$, $V_{CLK} = 0V$, $V_{ST1} = V_{ST2} = 0V$ or V_{DD} , $T_A = +25^\circ C$	-1		+1	μA
LOGIC SIGNALS (CLK, EN)						
Input Logic-High Voltage	V_{IH}		2			V
Input Logic-Low Voltage	V_{IL}				0.8	V

($V_{DD} = 8V$ to $36V$, $V_{EN} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$ unless otherwise noted, Typical values are at $T_A = +25^\circ C$ (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	$V_{CLK} = V_{EN} = 5.5V$ or $0V$	-1		+1	μA
FAULT Output Logic-Low Voltage	V_{OL}	$I_{FAULT} = 10mA$			1	V
FAULT Leakage Current	I_{LKGF}	$V_{FAULT} = 36V$, FAULT deasserted			10	μA
AC CHARACTERISTICS						
Switching Frequency	f_{SW}	$V_{CLK} = 0V$, measured at ST1/ST2 outputs	255		700	kHz
CLK Input Frequency	f_{EXT}	External clocking	200		2000	kHz
ST1/ST2 Duty Cycle	D_{TC}	Internal or external clocking, $f_{EXT} \leq 1000kHz$ (Note 4)	49	50	51	%
		External clocking, $f_{EXT} > 1000kHz$ (Note 4)	48	49	50	
ST1/ST2 Rise Time	t_{RISE}	ST1/ ST2 = 20% to 80% of V_{DD} , $R_L = 1k\Omega$, $C_L = 50pF$, Figure 1A			100	ns
ST1/ST2 Fall Time	t_{FALL}	ST1/ST2 = 80% to 20% of V_{DD} , $R_L = 1k\Omega$, $C_L = 50pF$, Figure 1A			100	ns
Crossover Dead Time	t_{DEAD}	$R_L = 200\Omega$, Figure 1B		30		ns
Watchdog Timeout	t_{WDOG}	(Note 5), $V_{DD} = 36V$	20	32	55	μs
Current-Limit Blanking Time	t_{BLANK}	Figure 2 , $V_{DD} = 36V$	0.73	1.2	2.0	ms
Current-Limit Autoretry Time	t_{RETRY}	Figure 2 , $V_{DD} = 36V$	23.4	38.4	64.0	ms
PROTECTION						
Thermal-Shutdown Threshold	T_{SHDN}			+160		$^\circ C$
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			10		$^\circ C$

Note 1: Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at $T_A = +25^\circ C$.

Note 2: If V_{DD} is greater than 27V, see the [Snubber](#) section.

Note 3: Guaranteed by design and simulation; not production tested.

Note 4: See the [Watchdog](#) section.

Test Circuits/Timing Diagrams

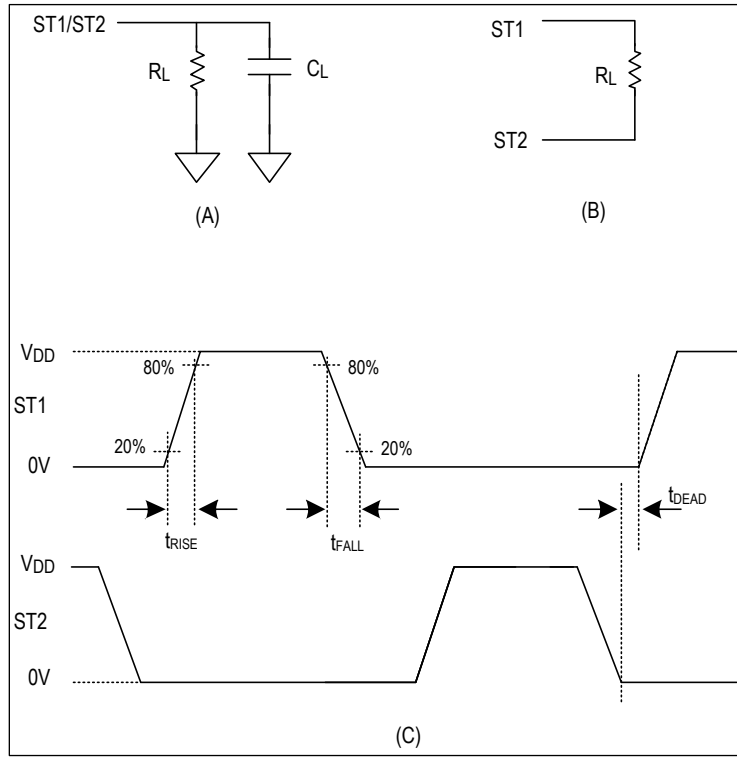


Figure 1. Test Circuits (A and B) and Timing Diagram (C) for Rise, Fall, and Dead Times

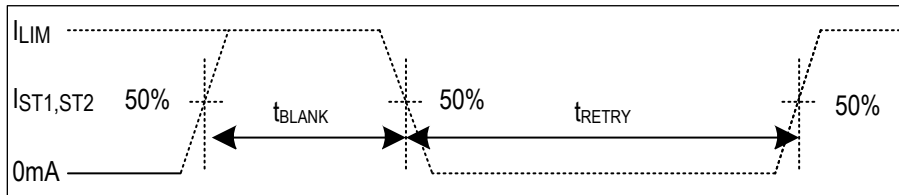
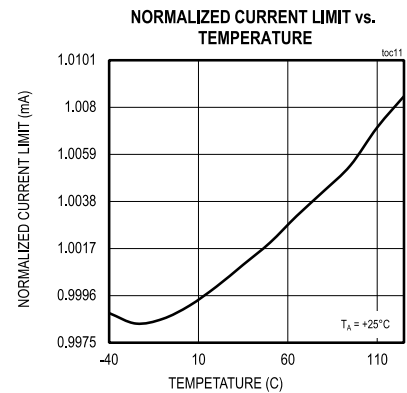
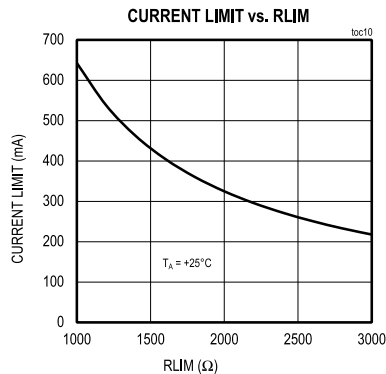
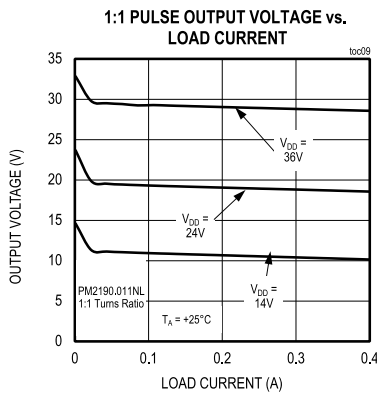
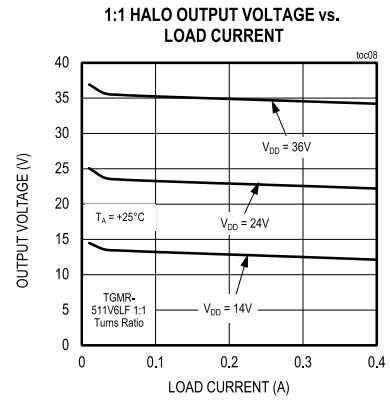
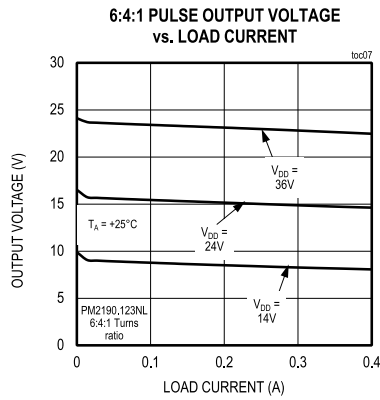
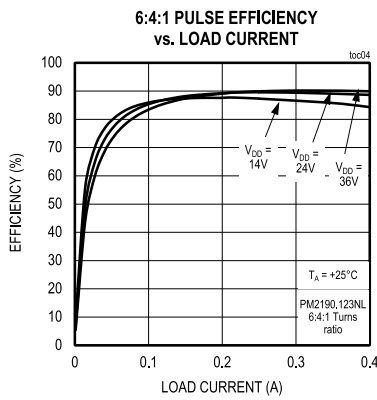
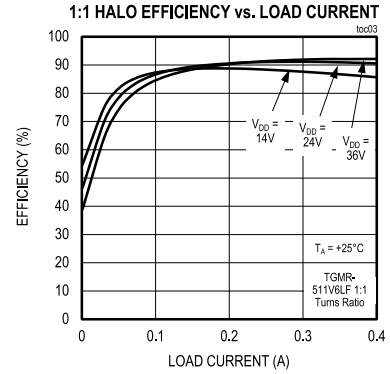
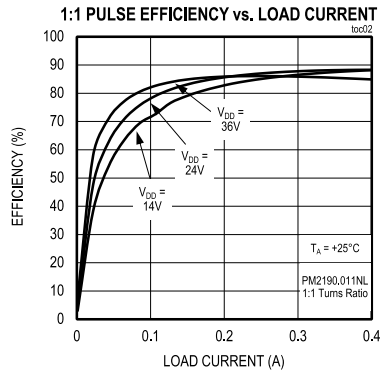
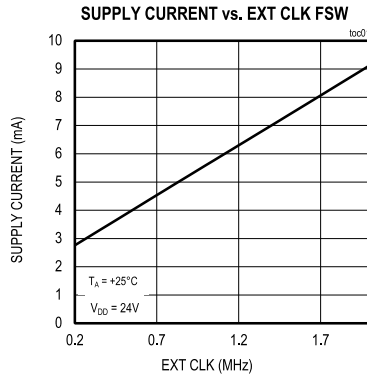


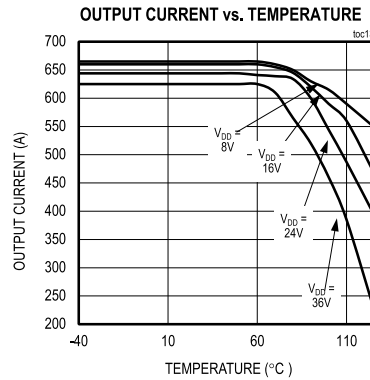
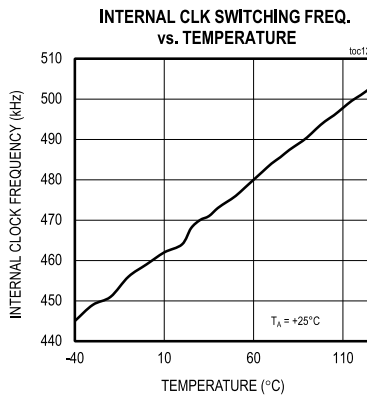
Figure 2. Timing Diagram for Current Limiting

Typical Operating Characteristics

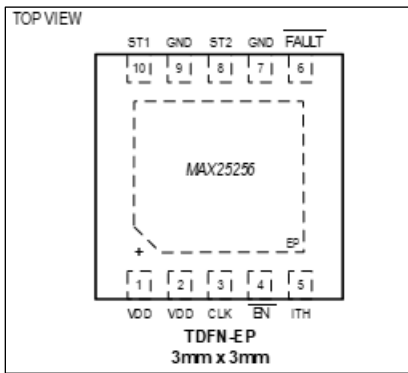
$V_{DD} = 24V$, $T_A = +25^\circ C$, unless otherwise stated



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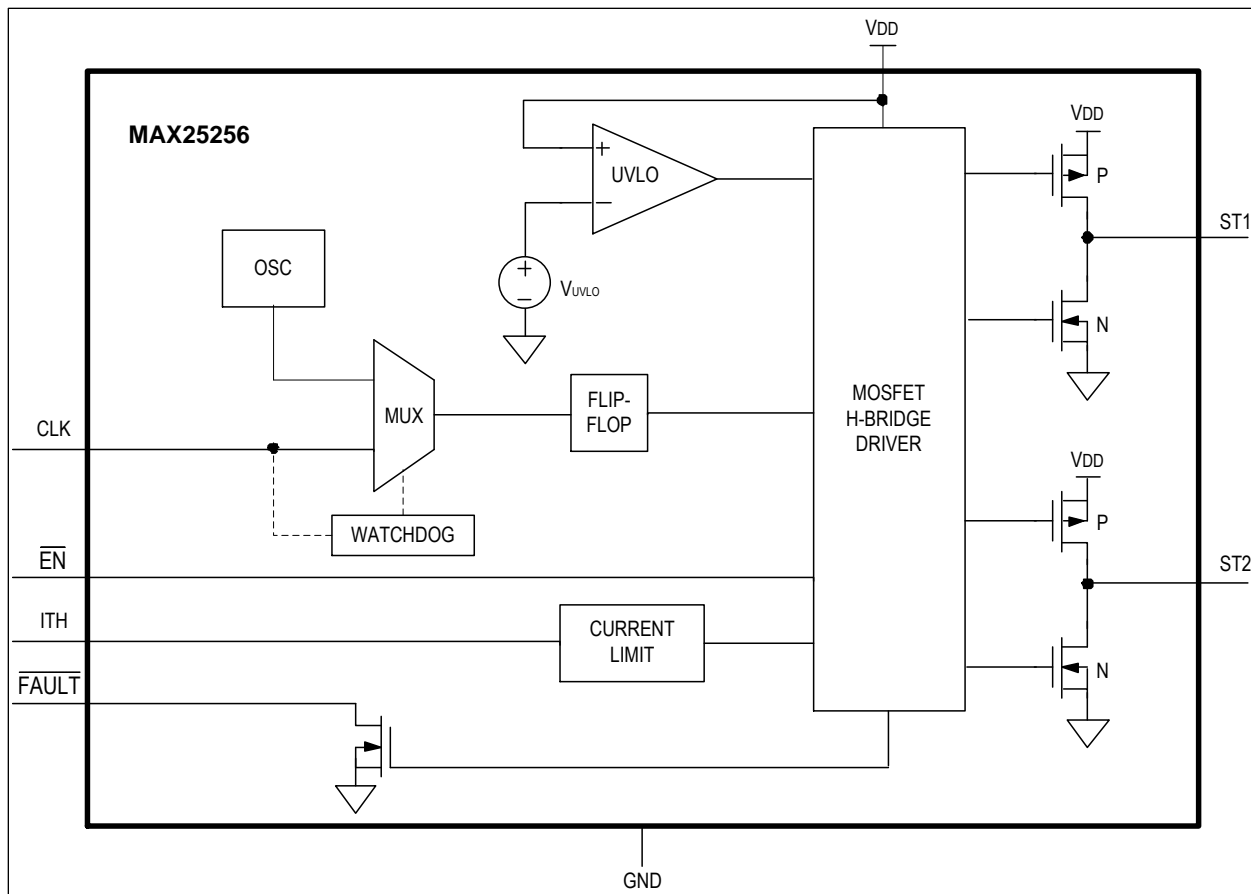
Pin Configurations



Pin Descriptions

PIN	NAME	FUNCTION
1,2	V_{DD}	Power Supply. Bypass V_{DD} to ground with a $1\mu F$ capacitor as close as possible to the device.
3	CLK	Clock Input. Connect CLK to GND to enable internal clocking. Apply a clock signal to CLK to enable external clocking.
4	\overline{EN}	Enable Input. Drive \overline{EN} low to enable the device. Drive \overline{EN} high to disable the device.
5	I_{TH}	Overcurrent Threshold Adjustment Input. Connect a resistor (R_{LIM}) from I_{TH} to GND to set the overcurrent threshold for the ST1 and ST2 outputs. Do not exceed 10pF of capacitance to GND on I_{TH} .
6	\overline{FAULT}	\overline{FAULT} Open-Drain Output. The fault open-drain transistor turns on when there is either an overtemperature or overcurrent condition.
7,9	GND	Ground
8	ST2	Transformer Drive Output 2
10	ST1	Transformer Drive Output 1
—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance; not intended as an electrical connection point.

Functional Diagrams



Detailed Description

The MAX25256 is an integrated primary-side controller and H-bridge driver for isolated power-supply circuits. The device contains an on-board oscillator, protection circuitry, and internal metal-oxide semiconductor field-effect transistors (MOSFETs) to provide up to 300mA of current to the primary winding of a transformer. The device can be operated using the internal oscillator or driven by an external clock to synchronize multiple MAX25256 devices and control EMI behavior. Regardless of the clock source being used, an internal flip-flop stage guarantees a fixed 50% duty cycle to prevent DC flow in the transformer as long as the period of the clock is constant.

The device operates from a wide single-supply voltage of 8V to 36V and includes UVLO for controlled startup. The device features break-before-make switching to prevent cross conduction of the H-bridge MOSFETs. An external resistor sets an overcurrent limit, allowing primary-side limiting of load currents on the transformer's secondary side. The thermal-shutdown circuitry provides additional protection against excessive power dissipation.

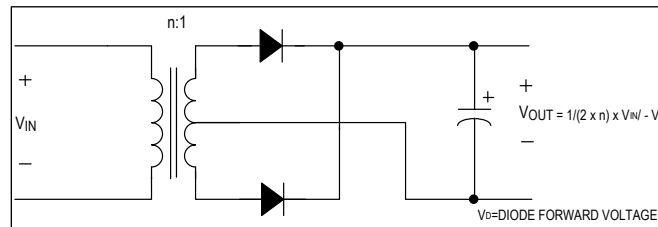
Power-Up and Undervoltage Lockout

The MAX25256 provides an undervoltage-lockout feature to both ensure a controlled power-up state and prevent operation before the oscillator has stabilized. On power-up and during normal operation if the supply voltage drops below V_{UVLO} , the undervoltage-lockout circuit forces the device into disable mode. The ST1 and ST2 outputs are high impedance in disable mode.

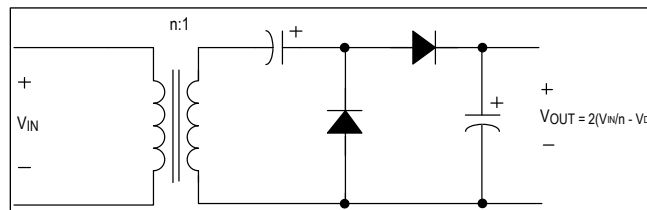
Isolated Power Supply

The MAX25256 allows a versatile range of secondary-side rectification circuits (see [Figure 3](#)). The primary-to-secondary transformer winding ratio can be chosen to adjust the isolated output voltage. The device delivers up to 300mA of current to the transformer with a supply up to +36V.

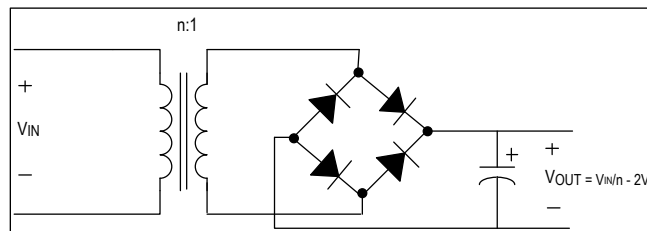
The MAX25256 provides the advantages of the H-bridge converter topology, including multiple isolated outputs, step-up/step-down or inverted output, relaxed filtering requirements, and low-output ripple.



(A) PUSH-PULL RECTIFICATION



(B) VOLTAGE DOUBLER



(C) FULL-WAVE RECTIFIER

Figure 3. Secondary-Side Rectification Topologies

Clock Source

Either the internal oscillator or an external clock provides the switching signal for the MAX25256. Connect CLK to ground to select the internal oscillator. Provide a clock signal to CLK to automatically select external clocking.

Internal Oscillator Mode

The MAX25256 includes an internal oscillator that drives the H-bridge when a watchdog timeout is detected on CLK. The outputs switch at 425kHz (typ) with a duty cycle of 50%, guaranteed by design, in the internal oscillator mode.

Transients on ST1/ST2 During t_{DEAD}

When the MAX25256 switches, there is a period of time when both ST1 and ST2 are high impedance to ensure that there are no shoot-through currents in the H-bridge. During this dead time, the voltage at these pins may temporarily exceed the absolute maximum ratings due to the inductive load presented by the transformer. This transient voltage does not damage the device.

Disable Mode

The MAX25256 provides a disable mode to reduce current consumption. The ST1 and ST2 outputs are high impedance in disable mode.

Watchdog

A stalled clock could cause excessive DC to flow through the primary winding of the transformer. The MAX25256 features an internal watchdog circuit to prevent damage from this condition. The internal oscillator provides the switching signal to the H-bridge whenever the period between edges on CLK exceeds the watchdog timeout period of 20µs (min).

External Clock Mode

The MAX25256 provides an external clock mode. When an external clock source is applied to CLK, the external clock drives the H-bridge. An internal flip-flop divides the external clock by two in order to generate a switching signal with a 50% duty cycle. As a result, the device outputs switch at one-half of the external clock frequency. The device switches on the rising edge of the external clock signal.

Note: There is a fixed asymmetric delay which reduces the ON-time by 10ns and hence the actual duty cycle observed at the output will be slightly lower than 50%, depending on the clock frequency.

Overcurrent Limiting

The MAX25256 limits the ST1/ST2 output current. Connect an external resistor (R_{LIM}) to I_{TH} to set the current limit. When the current reaches the limit for longer than the blanking time of 1.2ms (typ), the drivers are disabled and \overline{FAULT} is asserted low. The drivers are re-enabled after the autoretry time of 38.4ms (typ). If a continuous fault condition is present, the duty cycle of the fault current is approximately 3%.

To set the current-limit threshold, use the following equation:

$$R_{LIM}(k\Omega) = \frac{650}{I_{LIM}(mA)}$$

where I_{LIM} is the desired current threshold in the range of 215mA < I_{LIM} < 650mA (typ). For example, a 1kΩ resistor sets the current limit to 650mA. Use a 1% resistor for R_{LIM} for increased accuracy.

Ensure that the overcurrent threshold is set to at least twice the expected maximum operating current. For an expected maximum operating current of 300mA, set the I_{LIM} to 650mA. For an expected operating current of 100mA, set the I_{LIM} to 215mA.

Thermal Shutdown

The MAX25256 is protected from overtemperature damage by a thermal-shutdown circuit. When the junction temperature (T_J) exceeds +160°C, the device is disabled and \overline{FAULT} is asserted low. \overline{FAULT} stays low for the duration of an overtemperature fault. The device resumes normal operation when T_J falls below +150°C.

FAULT Output

The \overline{FAULT} output is asserted low whenever the device is disabled due to a fault condition. \overline{FAULT} is automatically deasserted when the device is enabled after the autoretry time following an overcurrent fault, resulting in \overline{FAULT} toggling during a continuous overcurrent condition. \overline{FAULT} is asserted for the entire duration of an overtemperature fault. \overline{FAULT} is an open-drain output.

Applications Information**Snubber**

For V_{DD} greater than 27V, use a simple resistor-capacitor (RC) snubber circuit on ST1 and ST2 to ensure that the peak voltage is less than 40V during switching ([Figure 4](#)). Recommended values for the snubber are $R = 91\Omega$ and $C = 330pF$.

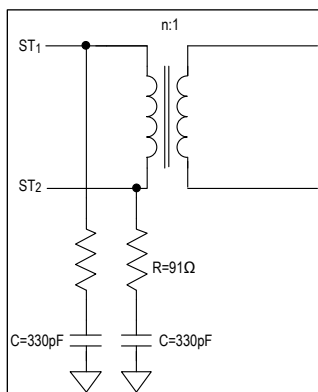


Figure 4. Output Snubber

Power Dissipation

The power dissipation of the device is approximated by:

$$P_D = (R_{OHL} \times I_{PRI}^2) + (I_{DD} \times V_{DD})$$

where R_{OHL} is the combined high-side and low-side on resistance of the internal field-effect transistors (FET) drivers, and I_{PRI} is the load current flowing through ST1 and ST2.

High-Temperature Operation

When the MAX25256 is operated under high ambient temperatures, the power dissipated in the package can raise the junction temperature close to thermal shutdown. Under such temperature conditions, the power dissipation should be held low enough so that the junction temperature observes a factor of safety margin. The maximum junction temperature should be held below +150°C. Use the package's thermal resistances to calculate the junction temperature. Alternatively, use the Maximum Output Current vs Temperature curves shown in the [Typical Operating Characteristics](#) section to determine the maximum ST1/ST2 load currents.

Hot Insertion

If the MAX25256 is inserted into a live backplane, it is possible to damage the device. Damage is caused by overshoot on V_{DD} exceeding the absolute maximum rating. Limit the transient input voltage to the MAX25256 with an external protection device.

Output Ripple Filtering

Output-voltage ripple can be reduced with a low-pass LC filter (see [Figure 5](#)). The component values shown give a cutoff frequency of 21.5kHz by the following equation:

$$f_{3dB} = \frac{1}{2\pi\sqrt{LC}}$$

Use an inductor with low DC resistance and sufficient saturation current rating to minimize the filter power dissipation.

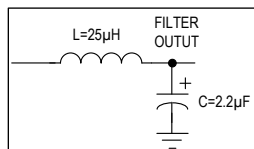


Figure 5. Output Ripple Filtering

Power Supply Decoupling

Bypass V_{DD} to ground with a 1μF ceramic capacitor as close as possible to the device.

Output Voltage Regulation

For many applications, the unregulated output of the MAX25256 meets the output-voltage tolerances. This configuration represents the highest efficiency possible with the device.

For applications requiring a regulated output voltage, Maxim provides several solutions. In the following examples, assume a tolerance of $\pm 10\%$ for the input voltage.

When the load currents on the transformer's secondary side are low, the output voltage can significantly increase. If operation under low-load currents is expected, output voltage limiting should be used to keep the voltage within the tolerance range of the subsequent circuitry. If the minimum output load current is less than approximately 5mA, connect a zener diode from the output node to ground as shown in [Figure 6](#) to limit the output voltage to a safe value.

Example 1: +24V to Isolated, +24V Output

In [Figure 6](#), the MAX25256 is used with a 1:1 transformer and a 4-diode bridge rectifier network (see [Figure 3C](#)) to supply +24V.

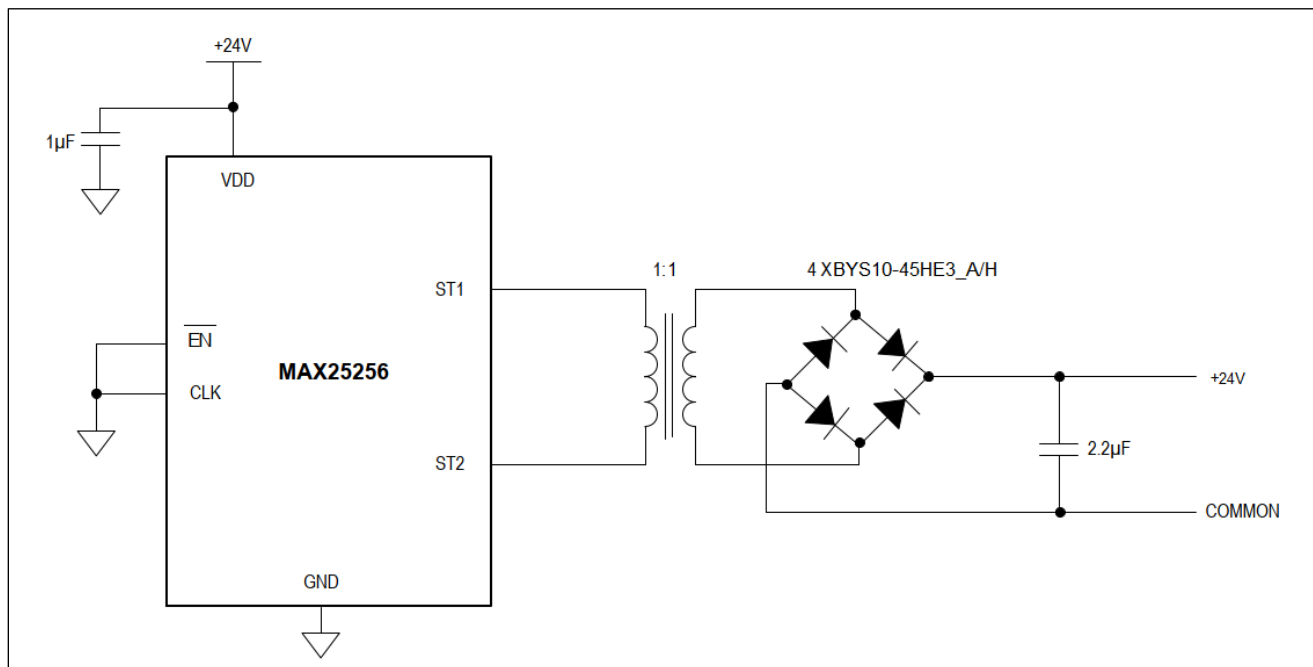


Figure 6. +24V to Isolated, +24V Output

Example 2: +24V to Isolated, +15V and -4V Output

In [Figure 7](#), the MAX25256 is used with a 6:4:1 center-tapped transformer and a 4-diode bridge rectifier network (see [Figure 3C](#)) to supply +15V and -4V outputs.

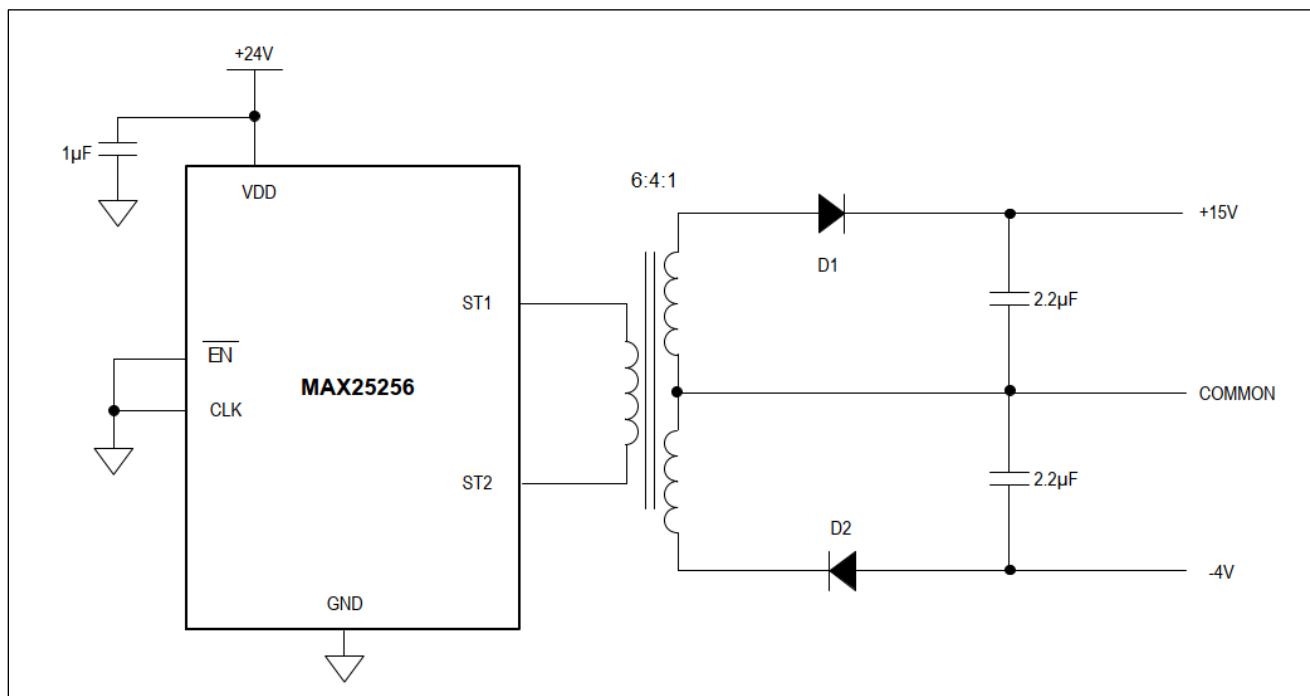


Figure 7. +24V to Isolated, +15V and -4V Output

PCB Layout Guidelines

As with all power-supply circuits, careful PCB layout is important to achieve low switching losses and stable operation. For thermal performance, connect the exposed pad to a solid copper ground plane. The traces from ST1 and ST2 to the transformer must be low-resistance and low-inductance paths. Place the transformer as close as possible to the MAX25256 using short, wide traces. When the device is operating with the internal oscillator, it is possible for high-frequency switching components on ST1 and ST2 to couple into the CLK circuitry through PCB parasitic capacitance. This capacitive coupling can induce duty-cycle errors in the oscillator, resulting in a direct current through the transformer. To ensure proper operation, ensure that CLK has a solid ground connection.

Exposed Pad

Ensure that the exposed pad has a solid connection to the ground plane for best thermal performance. Failure to provide a low thermal impedance path to the ground plane results in excessive junction temperatures when delivering maximum output power.

Component Selection

Input Bypass Capacitor

Bypass the supply pin to GND with a 1µF ceramic capacitor as close as possible to the device. The equivalent series resistance (ESR) of the input capacitors is not as critical as for the output filter capacitors. Typically, ceramic X7R capacitors are adequate.

Output Filter Capacitor

In most applications, the actual capacitance rating of the output filter capacitors is less critical than the capacitor's ESR. In applications sensitive to output-voltage ripple, the output filter capacitor must have low ESR. For optimal performance, the capacitance should meet or exceed the specified value over the entire operating temperature range. Capacitor ESR typically rises at low temperatures; however, OS-CON capacitors can be used at temperatures below 0°C to help reduce output-voltage ripple in sensitive applications. In applications where low output-voltage ripple is not critical, standard ceramic 0.1µF capacitors are sufficient.

Diode Selection

The high switching speed of the MAX25256 necessitates high-speed rectifiers. Ordinary silicon signal diodes such as 1N914 or 1N4148 can be used for low output-current levels (less than 50mA.) But at higher output-current levels, their reverse recovery times might degrade efficiency. At higher output currents, select low forward-voltage Schottky diodes to improve efficiency. Ensure that the average forward-current rating for the rectifier diodes exceeds the maximum load current of the circuit. For surface-mount applications, Schottky diodes such as the BYS10-45HE3_A/H, MBR5140, and MBR5340 are recommended.

Transformer Selection

Transformer selection for the MAX25256 can be simplified by use of the ET product design metric. The ET product relates the maximum allowable magnetic flux density in a transformer core to the voltage across a winding and switching period. Inductor magnetizing current in the primary winding changes linearly with time during the switching period of the device. Transformer manufacturers specify a minimum ET product for each transformer. The transformer's ET product must be larger than

$$ET = V_{DD} / (2 \times f_{SW})$$

where f_{SW} is the minimum switching frequency of the ST1/ST2 outputs (255kHz (min)) when the internal oscillator is used, or one-half of the clock frequency when an external clock source is used.

Choose a transformer with sufficient ET product in the primary winding to ensure that the transformer does not saturate during operation. Saturation of the magnetic core results in significantly reduced inductance of the primary, and therefore a large increase in the current flow. This can cause the current limit to be reached even when the load is not high.

For example, when the internal oscillator is used to drive the H-bridge, the required transformer ET product for an application with $V_{DD(MAX)} = 36V$ is 70.6V μ s. An application with $V_{DD(MAX)} = 8.8V$ has a transformer ET product requirement of 17.3V μ s.

In addition to the constraint on ET product, choose a transformer with a low DC-winding resistance. Power dissipation of the transformer due to the copper loss is approximated as follows:

$$P_{D_TX} = I_{LOAD}^2 \times (R_{PRI}/N^2 + R_{SEC})$$

where R_{PRI} is the DC winding resistance of the primary, and R_{SEC} is the DC winding resistance of the secondary.

In most cases, an optimum is reached when $R_{SEC} = R_{PRI}/N^2$. For this condition, the power dissipation is equal for the primary and secondary windings.

As with all power-supply designs, it is important to optimize efficiency. In designs incorporating small transformers, the possibility of thermal runaway makes low transformer efficiencies problematic. Transformer losses produce a temperature rise that reduces the efficiency of the transformer. The lower efficiency, in turn, produces an even larger temperature rise.

To ensure that the transformer meets these requirements under all operating conditions, the design should focus on the worst-case conditions. The most stringent demands on ET product arise for minimum input voltage, switching frequency, and maximum temperature and load current. Additionally, the worst-case values for transformer and rectifier losses should be considered.

The primary should be a single winding; however, the secondary can be center tapped, depending on the desired rectifier topology. In most applications, the phasing between primary and secondary windings is not significant. Half-wave rectification architectures are possible with the MAX25256; however, these are discouraged. If a net DC results due to an imbalanced load, the average magnetic flux in the core is increased. This reduces the effective ET product and can lead to saturation of the transformer core.

Transformers for use with the device are typically wound on a high-permeability magnetic core. To minimize radiated electromagnetic emissions, select a toroid, pot core, E/I/U core, or equivalent.

A list of recommended transformers can be found in the table below:

MANUFACTURER	P/N	TURNS RATIO	MANUFACTURER WEBSITE
Pulse	PM2190.011NL	1:1	https://www.pulseelectronics.com/
Pulse	PM2190.123NL	6:4:1	https://www.pulseelectronics.com/
Halo	TGMR-511V6LF	1:1	https://www.haloelectronics.com/

Low-Voltage Operation

The MAX25256 can be operated from a +8V supply by decreasing the turns ratio of the transformer, or by designing a voltage doubler circuit as shown in [Figure 3B](#).

Optimum performance at +8V is obtained with fewer turns on the primary winding since the ET product requirement is lower than for a +24V supply. However, any of the transformers for use with a +24V supply can operate properly with a +8V supply. For a given power level, the transformer currents are higher with a +8V supply than with a +24V supply. Therefore, the DC resistance of the transformer windings has a larger impact on the circuit efficiency.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX25256ATBA/V+	-40°C to +125°C	T1033+1C

+Denotes a lead(Pb)-free/RoHS-compliant package.

-Denotes a package containing lead(Pb).

/V denotes an automotive qualified part.

Devices are also available in a lead(Pb)-free/RoHS-compliant package.

Specify lead-free by adding "+" to the part number when ordering.

Devices are also available in tape-and-reel packaging. Specify tape and reel by adding "T" to the part number when ordering.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	04/21	Initial release	—

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