

## 267 MHz 1:2 3.3V HCSL/LVDS Fanout Buffer

### Features

- Two Differential Pairs of LVDS or HCSL Outputs
- Two Pairs of Differential Inputs Accept LVDS or HCSL Logic Levels
- 267 MHz Maximum Frequency
- Ultra-Low Phase Jitter:
  - 137 fs<sub>RMS</sub>, 200 MHz (12 kHz - 20 MHz)
  - 153 fs<sub>RMS</sub>, 156.25 MHz (12 kHz - 20 MHz)
  - 212 fs<sub>RMS</sub>, 100 MHz (12 kHz - 20 MHz)
- <2 ps Total Jitter (peak-to-peak), 200 MHz (BER = 10<sup>-12</sup>)
- 50 ps Output-to-Output Skew
- 3.3V ±5% Power Supply Operation
- -40°C to +85°C Operating Temperature
- Available in 16-pin (3 mm × 3 mm) QFN Lead-Free Package

### Applications

- Blade Servers
- Desktop Servers
- Workstations
- Storage Area Networks
- IP Routers and Switches
- Telecom and Datacom
- High Performance Computing

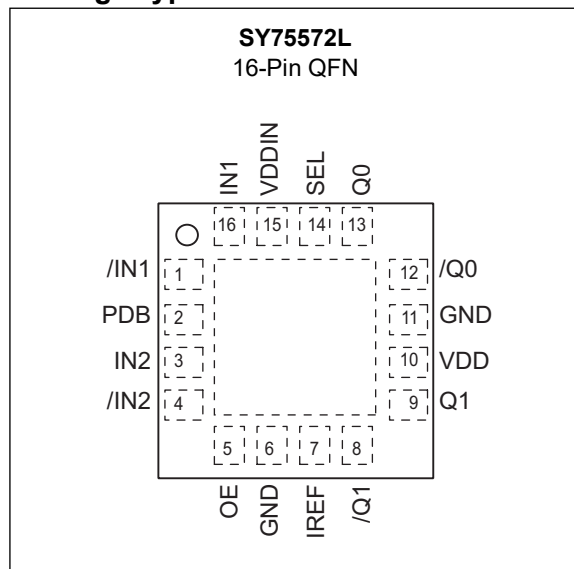
### General Description

The SY75572L is a high-speed, fully differential 1:2 clock fanout buffer with a 2:1 input MUX optimized to provide two identical output copies with 137 fs phase jitter and a maximum of 50 ps output-to-output skew. Designed to be used with PCI Express applications, the SY75572L accepts and outputs HCSL or LVDS logic levels.

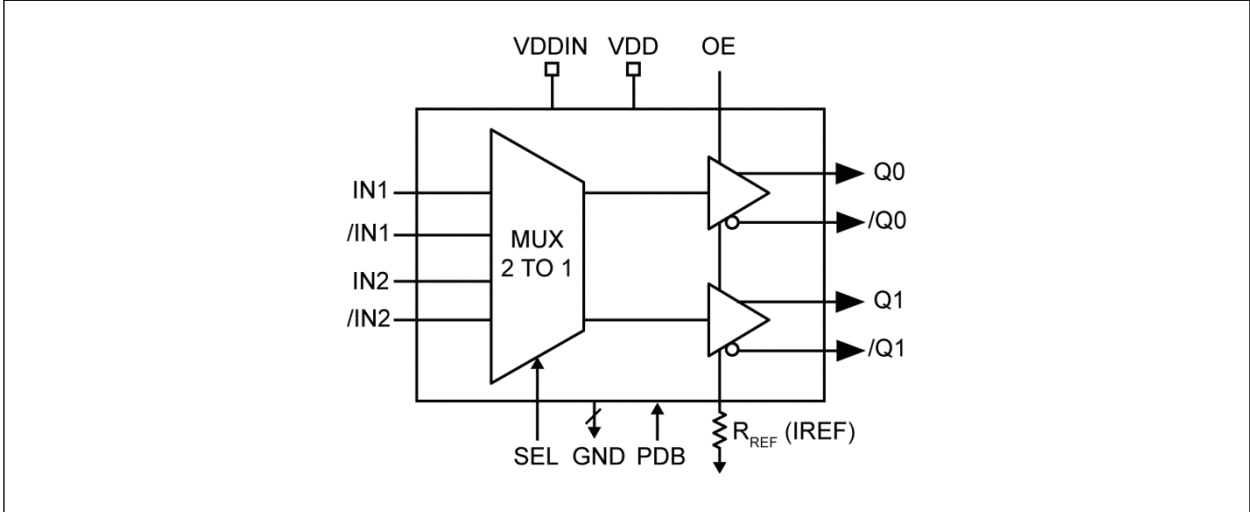
The SY75572L operates from a 3.3V ±5% power supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). It is available in a 16-pin QFN lead-free package.

The SY75572L is part of Microchip's high-speed, ultra-low jitter, PrecisionEdge™ product line. The SY75572L supports PCIe Gen1-Gen4 requirements.

### Package Type



Functional Block Diagram



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## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage, $V_{CC}$ , $V_{DDIN}$ .....	5.5V
Input Voltage, $V_{IN}$ .....	-0.5V to $V_{DDIN}$ +0.5V
ESD Protection (Input).....	2 kV

### Operating Ratings ††

Supply Voltage, $V_{DD}$ , $V_{DDIN}$ .....	3.135V to 3.465V
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**† Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

**†† Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

## DC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:**  $V_{DD} = V_{DDIN} = 3.135V$  to  $3.465V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise stated.  
 $R_{REF} = 475\Omega$ . (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage Range	$V_{DD}, V_{DDIN}$	3.135	3.3	3.465	V	—
Input Capacitance	$C_{IN}$	—	—	6	pF	—
Output Capacitance	$C_{OUT}$	—	—	5	pF	—
Pin Inductance	$L_{PIN}$	—	—	4	nH	—
Output Resistance	$R_{OUT}$	3	—	—	k $\Omega$	—
Pull up Resistance	$R_{PULL-UP}$	—	110	—	k $\Omega$	SEL, PDB, OE
Input High Voltage	$V_{IH}$	2	—	$V_{DDIN} + 0.3$	V	SEL, PDB, OE
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V	SEL, PDB, OE
Input High Voltage	$V_{IH}$	350	—	850	mV	HCSL, IN, /IN
Input Low Voltage	$V_{IL}$	-150	0	—	mV	HCSL, IN, /IN
Differential Input Voltage Range	$V_{IN}$	200	350	550	mV	LVDS, IN, /IN
Input Common Mode Voltage	$V_{INPUT\ OFFSET}$	1.125	1.25	1.375	V	LVDS, IN, /IN
Output High Voltage	$V_{OH}$	660	750	850	mV	HCSL
Output Low Voltage	$V_{OL}$	-150	0	27	mV	HCSL
Crossing Point Voltage <a href="#">Note 2</a> , <a href="#">Note 3</a>	$V_{CROSS}$	250	350	550	mV	Absolute
Variation of Crossing Point Voltage <a href="#">Note 2</a> , <a href="#">Note 3</a> , <a href="#">Note 4</a>	$V_{CROSS\_VARIATION}$	—	—	140	mV	Variation over all edges
Power Supply Current For $V_{DD} + V_{DDIN}$	$I_{DD}$	—	42	60	mA	50 $\Omega$ , 2 pF
		—	—	0.4		No load, PDB = Low
		—	—	20		OE = Logic Low
Input Leakage Current <a href="#">Note 5</a>	$I_{IL}$	-5	—	5	$\mu A$	$0 < V_{IN} < V_{DDIN}$

**Note 1:** The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

**2:** Test setup is  $R_L = 50\Omega$  with 2 pF,  $R_{REF} = 475\Omega \pm 1\%$ .

**3:** Measurement taken from Q and /Q.

**4:** Measured at the crossing point where instantaneous voltages of Q and /Q are equal.

**5:** Inputs with pull-up/pull-down resistances are not included.

## AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{DD} = V_{DDIN} = 3.135V$ to $3.465V$ , $T_A = -40^{\circ}C$ to $+85^{\circ}C$ , unless otherwise stated. (Note 1)						
Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Frequency	$f_{MAX}$	—	—	267	MHz	HCSL
		—	—	100		LVDS
Propagation Delay	$t_{PD}$	—	2	3	ns	Note 2
Output-to-Output skew	$t_{SKEW}$	—	—	50	ps	Note 3, Note 4
Output Rise/Fall Times 0.175V to 0.525V / 0.525V to 0.175V	$t_r, t_f$	150	350	700	ps	At full output swing. 50 $\Omega$ , 2 pF
Rise/Fall Time Variation	$t_{r/f\_VAR}$	—	—	125	ps	At full output swing. 50 $\Omega$ , 2 pF
Phase Jitter	$t_{JITTER}$	—	137	—	$f_{RMS}$	At 200 MHz
		—	153	—	$f_{RMS}$	At 156.25 MHz
		—	212	—	$f_{RMS}$	At 100 MHz
Total Jitter	$t_{T\_JITTER}$	—	2	—	ps	BER = $10^{-12}$ , $T_{DJ} = 0$ , at 200 MHz
Output Enable Time	$t_{OE\_ENABLE}$	—	2	—	$\mu s$	All outputs
Output Disable Time	$t_{OE\_DISABLE}$	—	10	—	ns	All outputs
Duty Cycle	$t_{DCY}$	45	50	55	%	—

- Note 1:** The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium as been established.
- 2:** Measured from the differential input crossing point to the differential output crossing point.
- 3:** Output-to-output skew is the difference in time between outputs, receiving data from the same input, for the same temperature, voltage, and transition.
- 4:** This parameter is defined in accordance with JEDEC Standard 65.

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**TEMPERATURE SPECIFICATIONS**

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Operating Temperature Range	$T_A$	-40	—	+85	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature Range	$T_S$	-65	—	+150	°C	—
<b>Package Thermal Resistance (Note 1)</b>						
16-Pin QFN	$\theta_{JA}$	—	59	—	°C/W	Still-Air
	$\psi_{JB}$	—	38	—	°C/W	Junction-to-board

**Note 1:** Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.  $\psi_{JB}$  and  $\theta_{JA}$  values are determined for a 4-layer board in still-air number, unless otherwise stated. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	/IN1	HCSSLVDS inverted input 1.
2	PDB	PDB = 0 powers down the chip and tri-states outputs. The pin is attached to an internal pull-up resistor.
3	IN2	HCSSLVDS input 2.
4	/IN2	HCSSLVDS inverted input 2.
5	OE	Tri-state outputs. High = enable outputs. Low = disable outputs. Internal pull-up resistor, outputs are enabled by default.
6	GND	Ground.
7	IREF	External resistor $R_{REF}$ between pin IREF and GND controls reference current.
8	/Q1	Inverted Output 1.
9	Q1	Non-inverted Output 1.
10	VDD	3.3V power supply.
11	GND	Ground.
12	/Q0	Inverted Output 0.
13	Q0	Non-inverted Output 0.
14	SEL	SEL = 0 propagates IN2, /IN2 to outputs. SEL = 1 propagates IN1, /IN1 to outputs. Internal pull-up resistors, IN1, /IN1 is selected by default.
15	VDDIN	3.3V power supply.
16	IN1	HCSSLVDS input 1.

## 3.0 JITTER ANALYSIS

Jitter is defined as the deviation of a signal from its ideal position. Phase noise is the presence of signal energy at frequencies other than the carrier. Random jitter has a Gaussian distribution and is specified as an RMS unit, which is one standard deviation of the distribution. Since Gaussian distribution is unbounded in an infinite sample, no communication system can be completely error free. Instead, communication links are rated with a maximum bit error rate (BER), which is typically around  $10^{-12}$  for high-speed communication equipment. Achieving a desired BER requires accounting for a number of standard deviations of random noise by using the appropriate value for N (see [Table 3-1](#)) in the formula in [Equation 3-1](#).

If routing clock signals, the deterministic jitter is usually negligible and the  $T_J$  is dominated by the random jitter. Calculating  $T_J$  from  $R_J$  using [Equation 3-1](#) gives the values in [Table 3-1](#).

**TABLE 3-1: STANDARD DEVIATIONS OF RANDOM NOISE**

BER	N	$R_J$ at 200 MHz	$T_J$ at 200 MHz
$10^{-10}$	12.723	137fs <sub>RMS</sub>	1.743 ps
$10^{-11}$	13.412	137fs <sub>RMS</sub>	1.837 ps
$10^{-12}$	14.069	137fs <sub>RMS</sub>	1.927 ps
$10^{-13}$	14.698	137fs <sub>RMS</sub>	2.013 ps

**EQUATION 3-1:**

$$T_J = N \times R_J + D_J$$

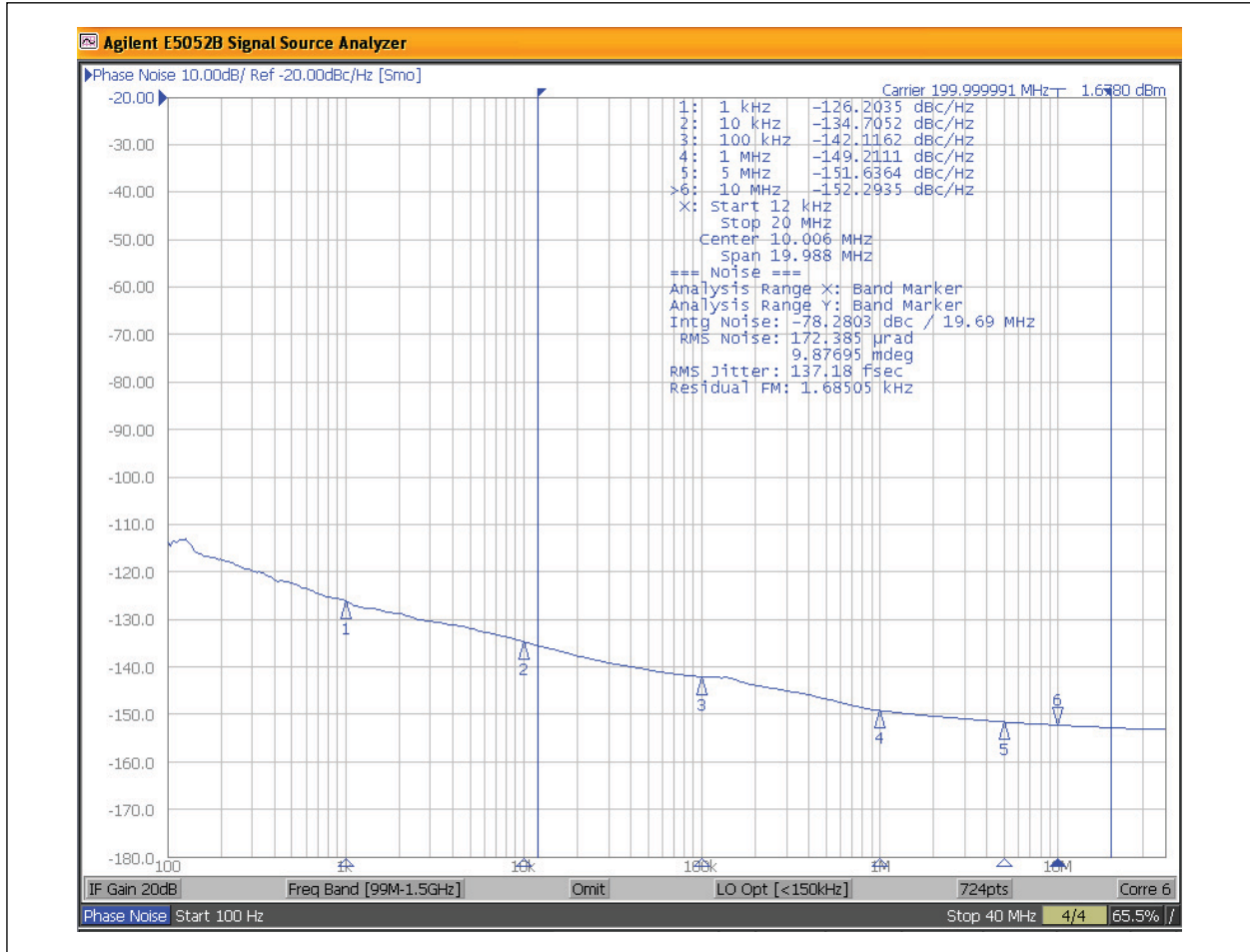
Where:

$T_J$  = Total jitter

$R_J$  = Random jitter

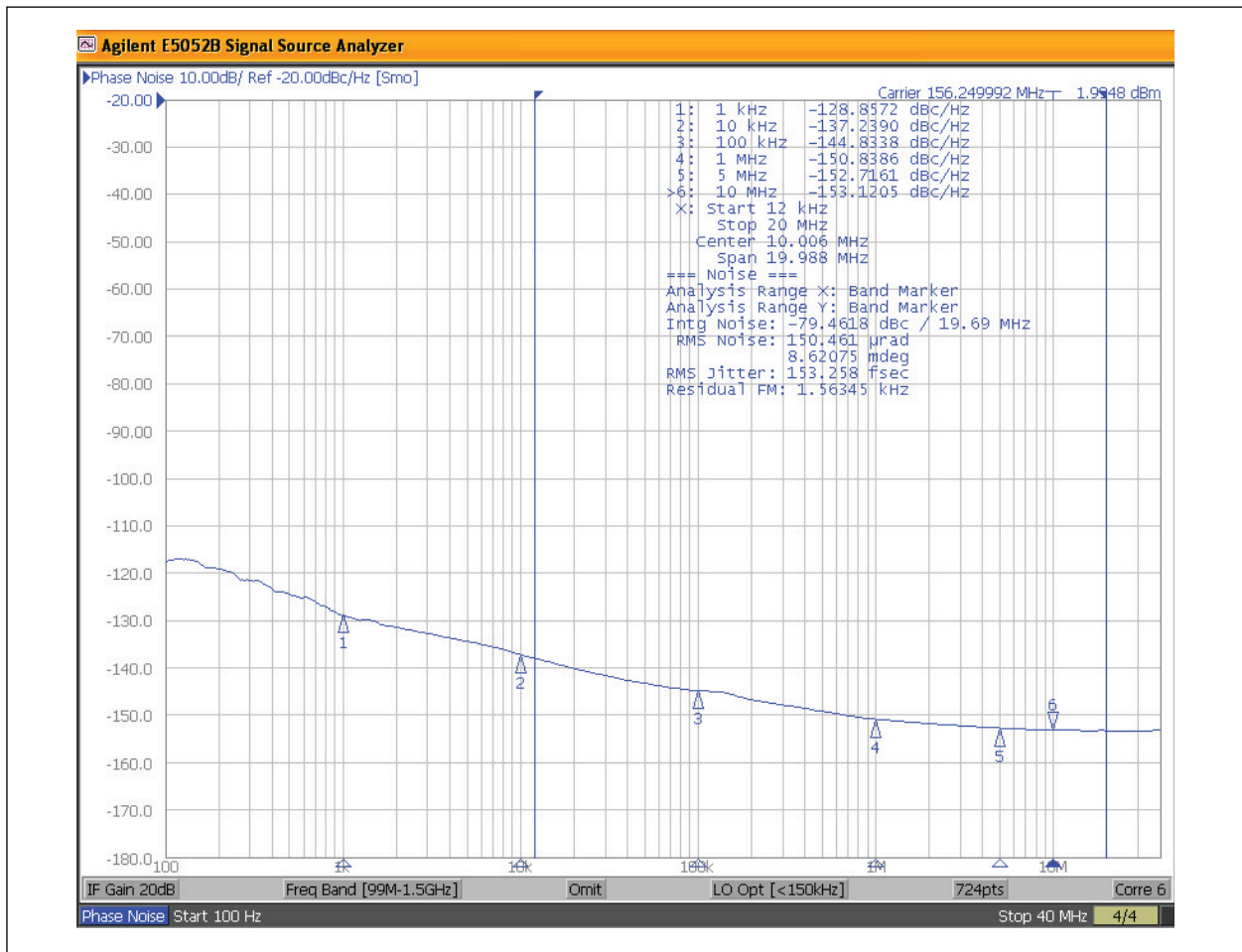
$D_J$  = Deterministic jitter

4.0 PHASE NOISE PLOTS

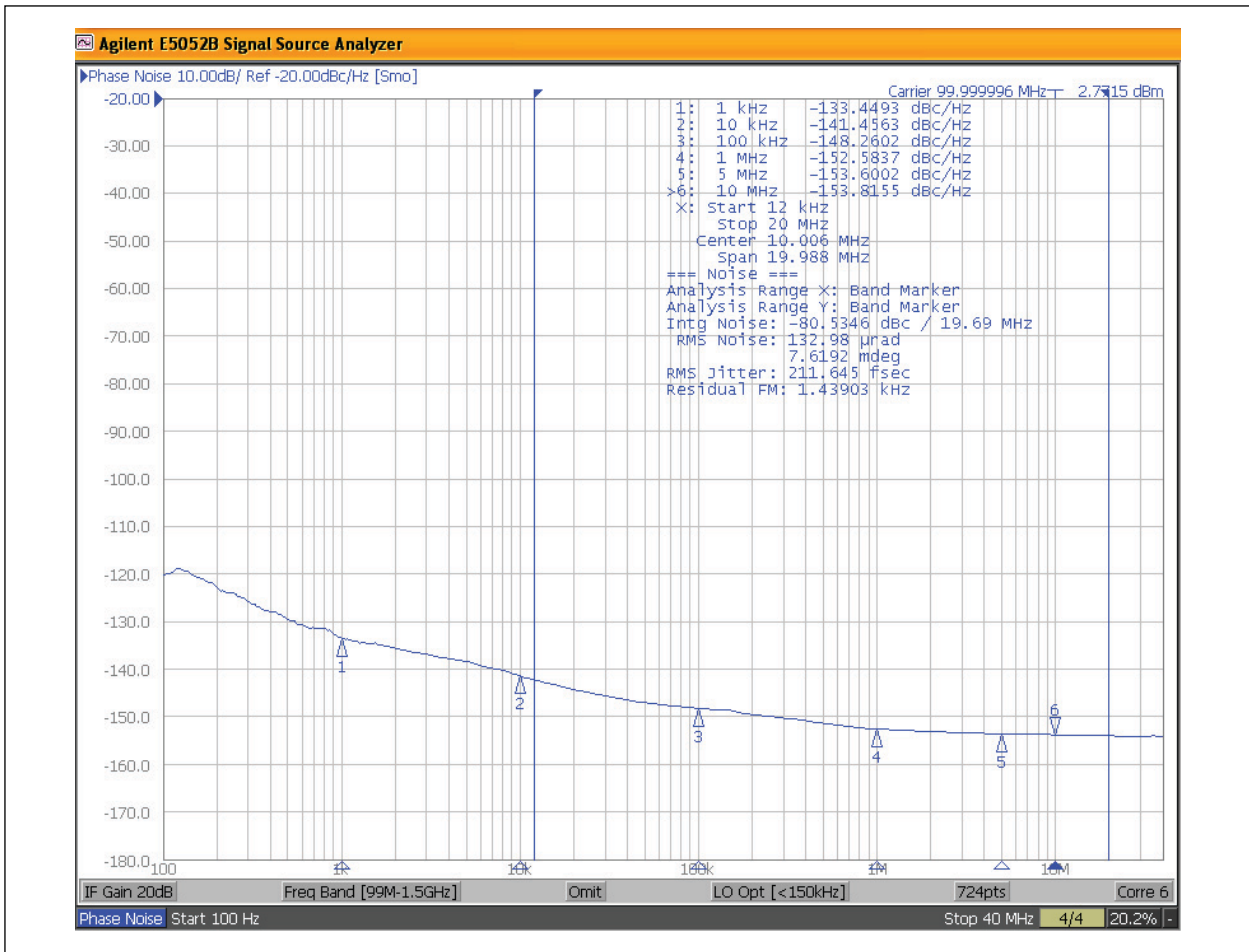


**FIGURE 4-1:** Phase Jitter = 137 fsRMS, 200 MHz Carrier Frequency; Integration Range: 12 kHz - 20 MHz.



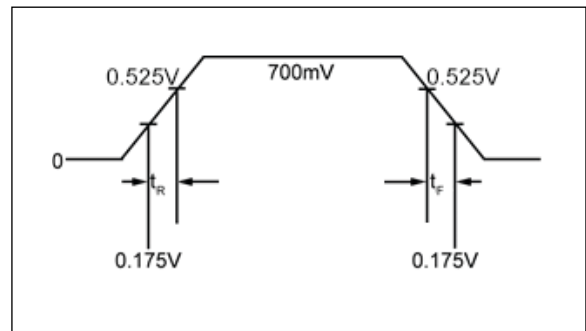
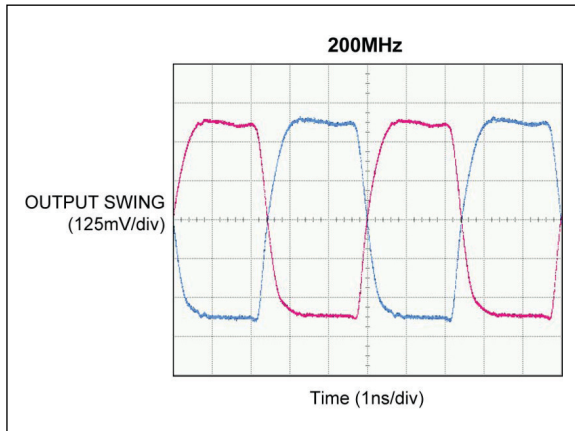
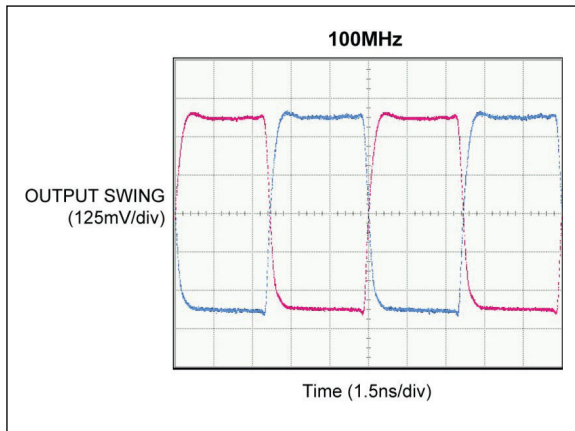


**FIGURE 4-2:** Phase Jitter = 153 fsRMS, 156.25 MHz Carrier Frequency;  
 Integration Range: 12 kHz - 20 MHz.

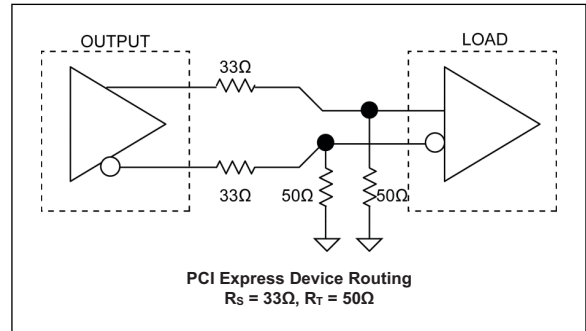


**FIGURE 4-3:** Phase Jitter = 212 fs<sub>RMS</sub>, 100 MHz Carrier Frequency; Integration Range: 12 kHz - 20 MHz.

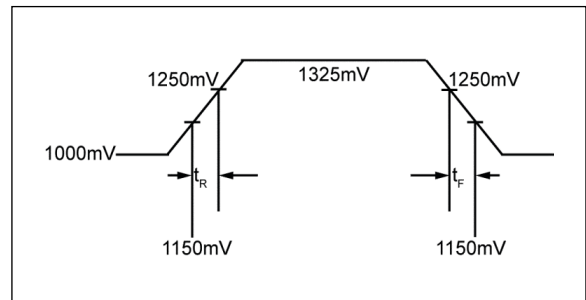
## 5.0 FUNCTIONAL CHARACTERISTICS



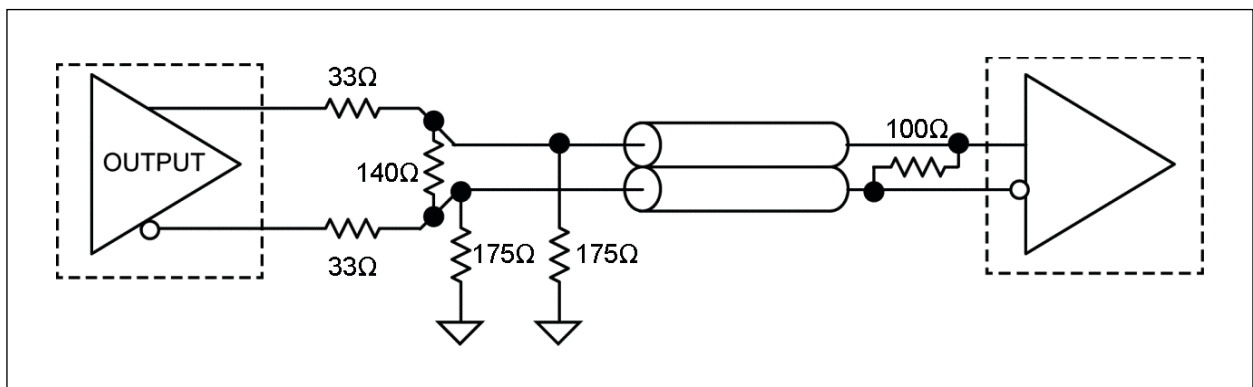
**FIGURE 5-1:** HCSL Waveform.



**FIGURE 5-2:** HCSL Interface Application.



**FIGURE 5-3:** LVDS Waveform.

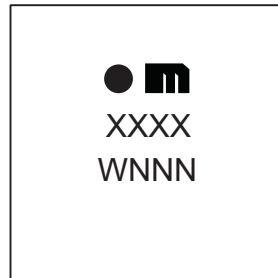


**FIGURE 5-4:** LVDS Interface Application.

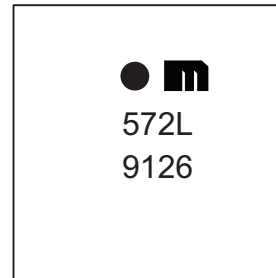
## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

16-Lead QFN\*



Example



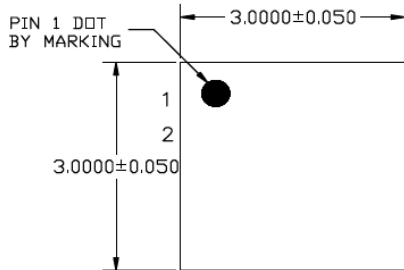
<b>Legend:</b>	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar ( ¯ ) and/or Overbar ( ¯ ) symbol may not be to scale.	

## 16-Lead QFN Package Outline and Recommended Land Pattern

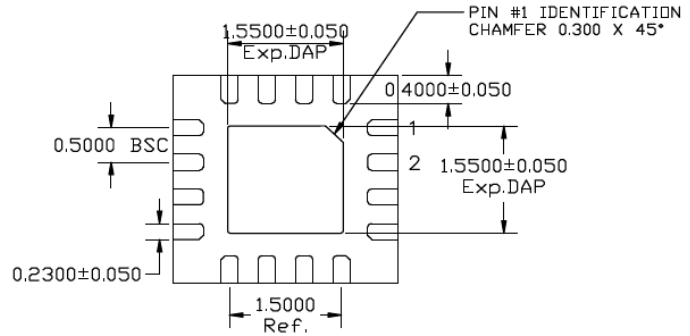
**TITLE**

16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

<b>DRAWING #</b>	QFN33-16LD-PL-1	<b>UNIT</b>	MM
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TOP VIEW  
NOTE: 1, 2, 3



BOTTOM VIEW  
NOTE: 1, 2, 3



SIDE VIEW  
NOTE: 1, 2, 3

**NOTE:**

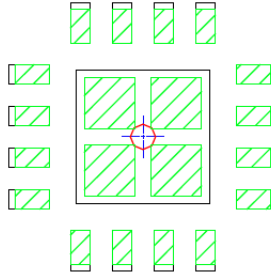
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

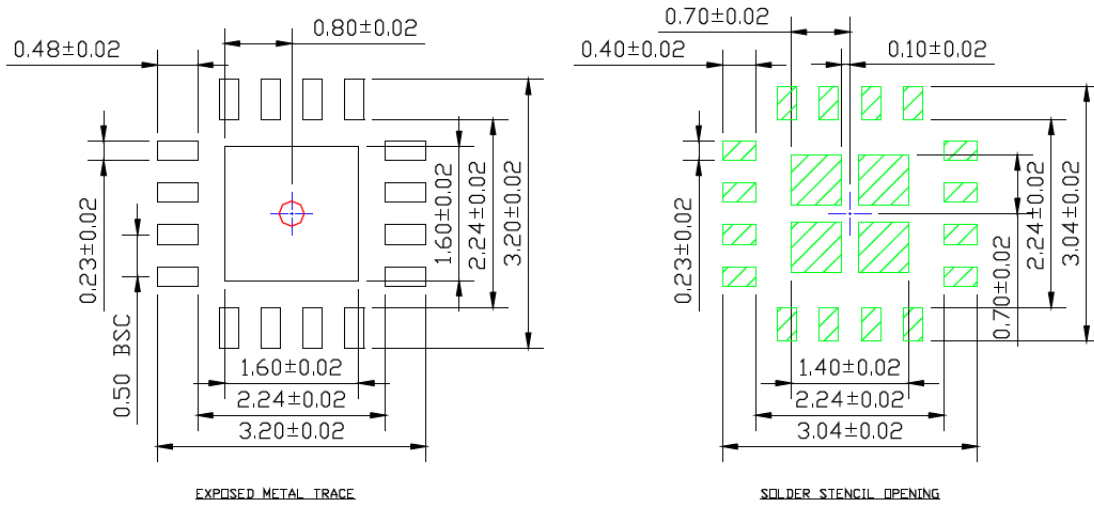
POD-Land Pattern drawing # QFN33-16LD-PL-1

## RECOMMENDED LAND PATTERN

NOTE: 4, 5



STACKED-UP



Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

## APPENDIX A: REVISION HISTORY

### Revision A (March 2022)

- Converted Micrel document SY75572L to Microchip data sheet template DS20006669A.
- Minor text changes throughout.

### Revision B (May 2023)

- Updated HCSSL Input High and Low Voltage information in the [DC Electrical Characteristics](#) table.

**NOTES:**



## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART #.	X	X	X	XX			
Device	Supply Voltage Range	Package	Junction Temperature Range	Special Processing			
<b>Device:</b>	SY75572:	2.5V/3.3V, 2.5 GHz Differential Two-Channel Precision CML Delay Line					
<b>Supply Voltage:</b>	L	=	3.3V				
<b>Package:</b>	M	=	16-Lead QFN				
<b>Temperature Range:</b>	G	=	-40°C to +85°C (NiPdAu Lead Free)				
<b>Special Processing:</b>	<blank>	=	100/Tube				
	<T/R>	=	1,000/Reel				

<b>Examples:</b>					
a)	SY75572,	3.3V	Output	SY75572LMG:	
	16-Lead	QFN,	-40°C	to	+85°C
	Temperature Range, 100/Tube				
b)	SY75572,	3.3V	Output	SY75572LMG-TR:	
	16-Lead	QFN,	-40°C	to	+85°C
	Temperature Range, 1,000/Reel				
<b>Note 1:</b>	Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.				

**NOTES:**

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