

# ESD8116

## ESD Protection Diode

### Low Capacitance Array for High Speed Data Lines

The ESD8116 surge protection is specifically designed to protect USB 3.0/3.1 interfaces from ESD. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow-through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines.

#### Features

- Low Capacitance (0.35 pF Max, I/O to GND)
- Protection for the Following IEC Standards:  
IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- USB 3.0/3.1
- Display Port

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T <sub>L</sub>	260	°C
IEC 61000-4-2 Contact (ESD) IEC 61000-4-2 Air (ESD)	ESD	±15	kV
		±15	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



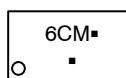
ON Semiconductor®

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#### MARKING DIAGRAM



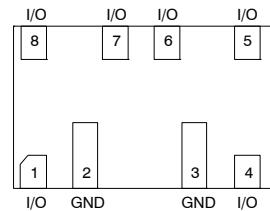
UDFN8  
CASE 517CX



6C = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN CONFIGURATION



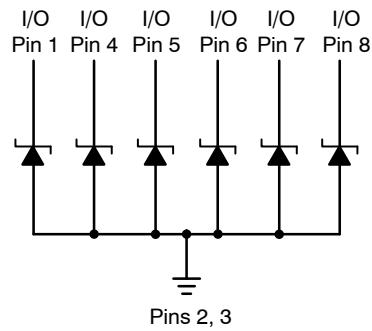
#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
ESD8116MUTAG	UDFN8 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

See Application Note AND8308/D for further description of survivability specs.

## ESD8116



Note: Common GND – Only Minimum of 1 GND connection required

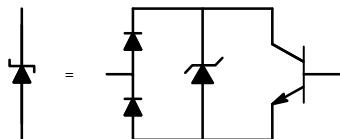


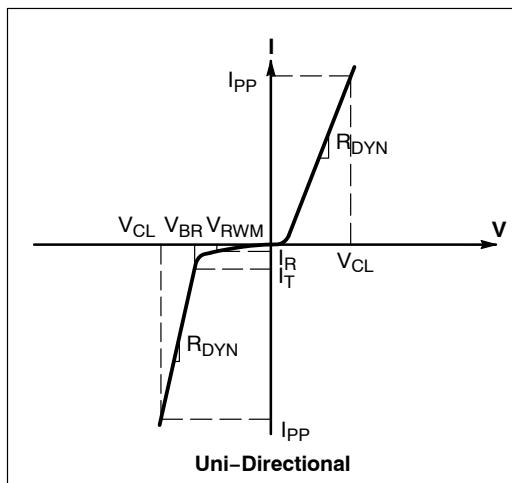
Figure 1. Pin Schematic

## ELECTRICAL CHARACTERISTICS

(T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter
I <sub>PP</sub>	Maximum Peak Pulse Current
V <sub>C</sub>	Clamping Voltage @ I <sub>PP</sub>
V <sub>RWM</sub>	Working Peak Reverse Voltage
I <sub>R</sub>	Maximum Reverse Leakage Current @ V <sub>RWM</sub>
V <sub>BR</sub>	Breakdown Voltage @ I <sub>T</sub>
I <sub>T</sub>	Test Current
R <sub>DYN</sub>	Dynamic Resistance

\*See Application Note AND8308/D for detailed explanations of datasheet parameters.

ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V <sub>RWM</sub>	I/O Pin to GND			3.3	V
Breakdown Voltage	V <sub>BR</sub>	I <sub>T</sub> = 1 mA, I/O Pin to GND	4.0	5.0		V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 3.3 V, I/O Pin to GND			1.0	µA
Clamping Voltage (Note 1)	V <sub>C</sub>	IEC61000-4-2, ±8 kV Contact	See Figures 2 and 3			V
Clamping Voltage TLP (Note 2) See Figures 6 through 9	V <sub>C</sub>	I <sub>PP</sub> = 8 A      } IEC 61000-4-2 Level 2 equivalent I <sub>PP</sub> = -8 A      } (±4 kV Contact, ±4 kV Air)  I <sub>PP</sub> = 16 A      } IEC 61000-4-2 Level 4 equivalent I <sub>PP</sub> = -16 A      } (±8 kV Contact, ±15 kV Air)		8.5 -4.5		V
Dynamic Resistance	R <sub>DYN</sub>	I/O Pin to GND GND to I/O Pin		0.36 0.44		Ω
Junction Capacitance	C <sub>J</sub>	V <sub>R</sub> = 0 V, f = 1 MHz between I/O Pins and GND V <sub>R</sub> = 0 V, f = 1 MHz between I/O Pins V <sub>R</sub> = 0 V, f = 1 MHz, T <sub>A</sub> = 65°C between I/O Pins and GND		0.30 0.15 0.37	0.35 0.20 0.47	pF

1. For test procedure see Figures 4 and 5 and application note AND8307/D.

2. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.

TLP conditions: Z<sub>0</sub> = 50 Ω, t<sub>p</sub> = 100 ns, t<sub>r</sub> = 4 ns, averaging window; t<sub>1</sub> = 30 ns to t<sub>2</sub> = 60 ns.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

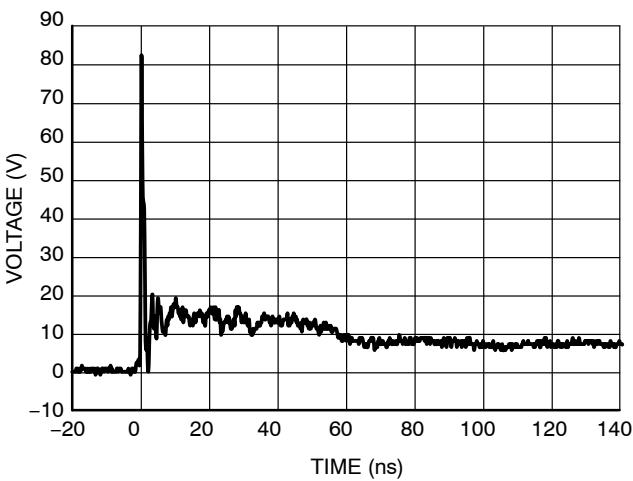


Figure 2. IEC61000-4-2 +8 kV Contact Clamping Voltage

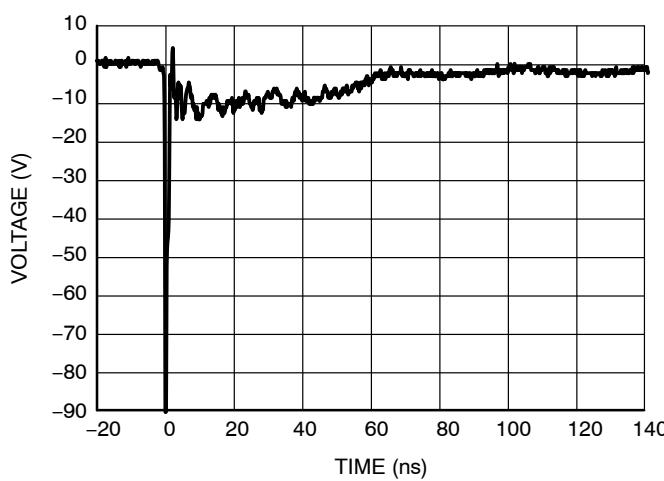


Figure 3. IEC61000-4-2 -8 kV Contact Clamping Voltage

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

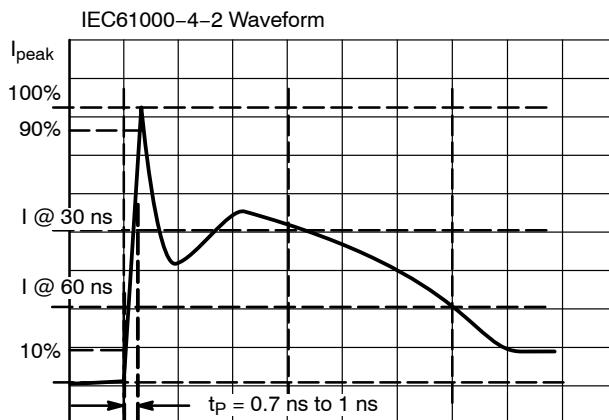


Figure 4. IEC61000-4-2 Spec

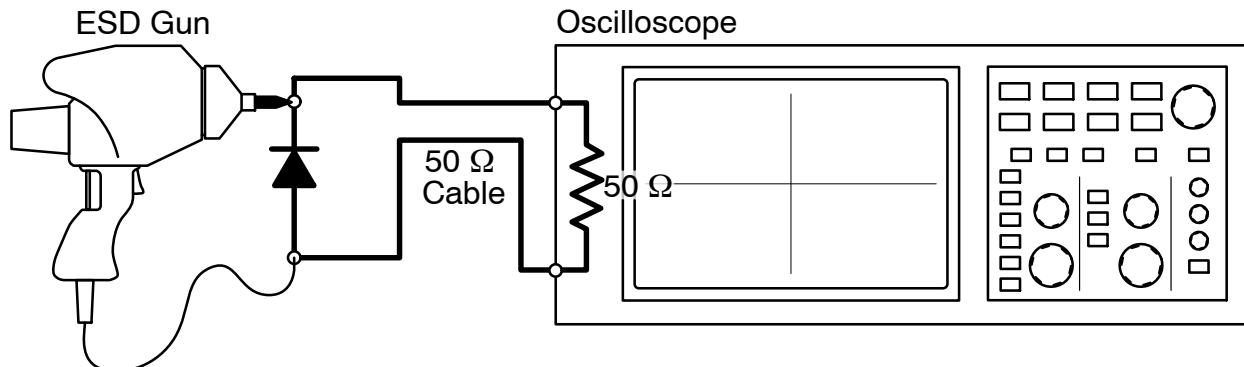


Figure 5. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8307/D – Characterization of ESD Clamping Performance.

#### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

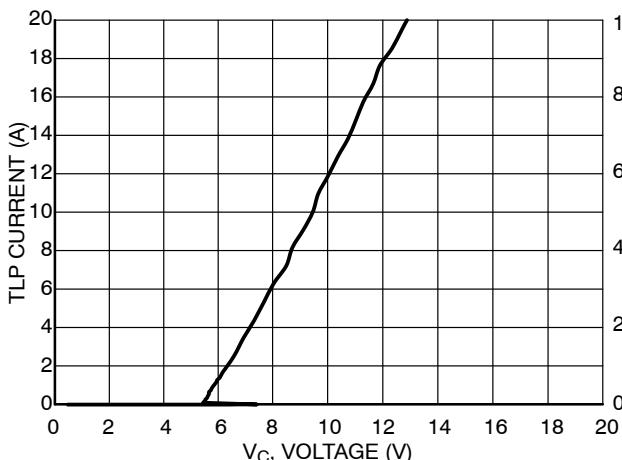


Figure 6. Positive TLP I-V Curve

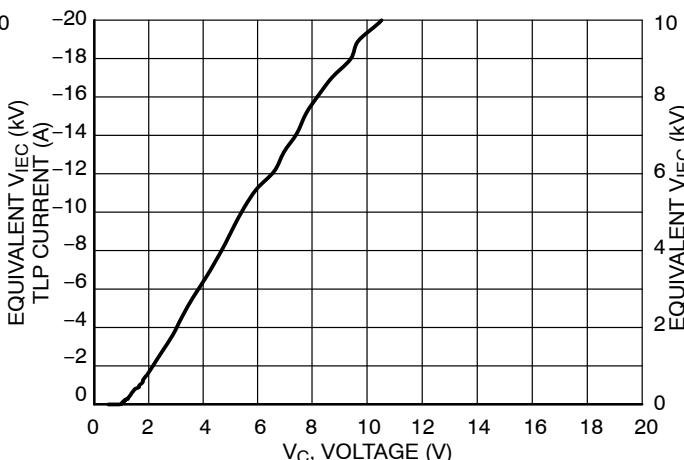


Figure 7. Negative TLP I-V Curve

NOTE: TLP parameter:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 300 \text{ ps}$ , averaging window:  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ .  $V_{IEC}$  is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000-4-2 waveform at  $t = 30 \text{ ns}$  with  $2 \text{ A/kV}$ . See TLP description below for more information.

#### Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

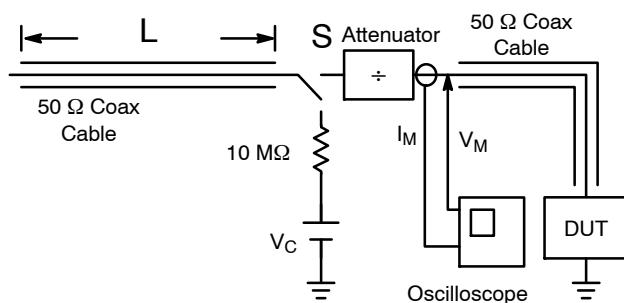


Figure 8. Simplified Schematic of a Typical TLP System

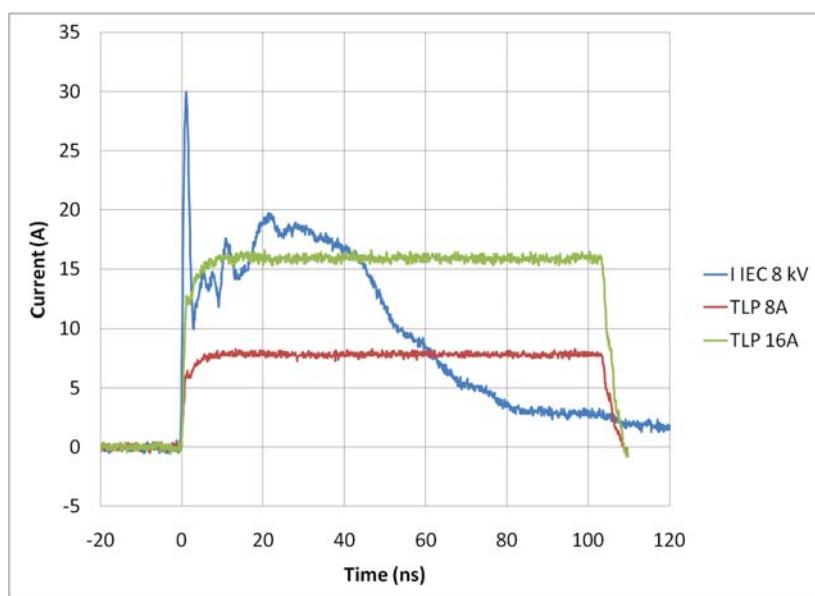


Figure 9. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

# ESD8116

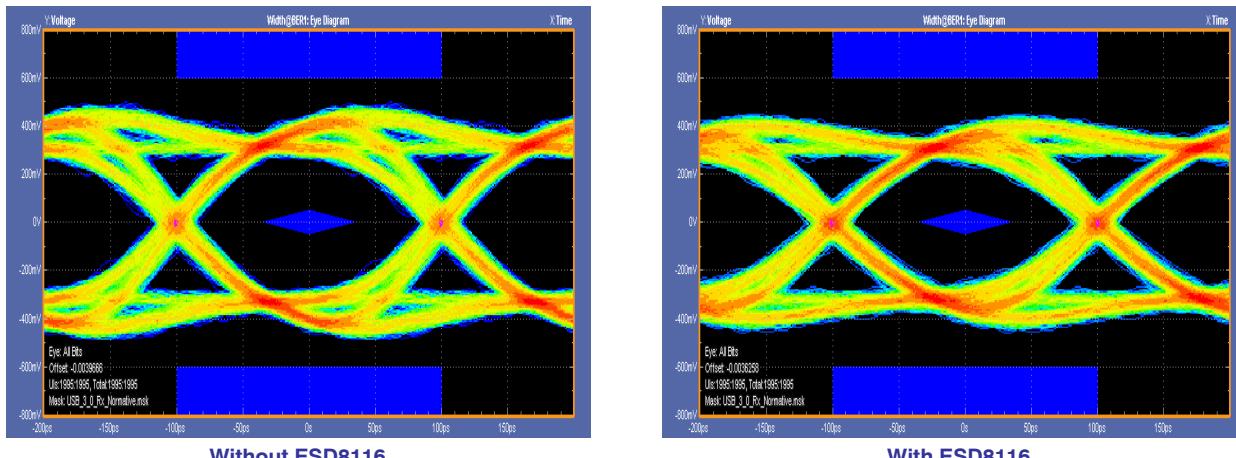
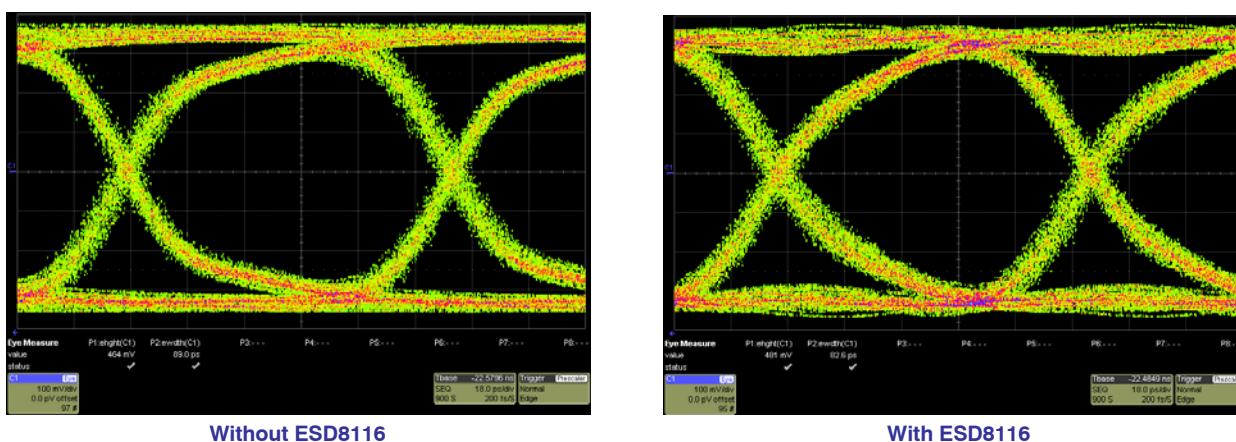


Figure 10. USB 3.0 Eye Diagram with and without ESD8116. 5 Gb/s



Without ESD8116

With ESD8116

Figure 11. USB 3.1 Eye Diagram with and without ESD8116. 10 Gb/s

See application note AND9075/D for further description of eye diagram testing methodology.

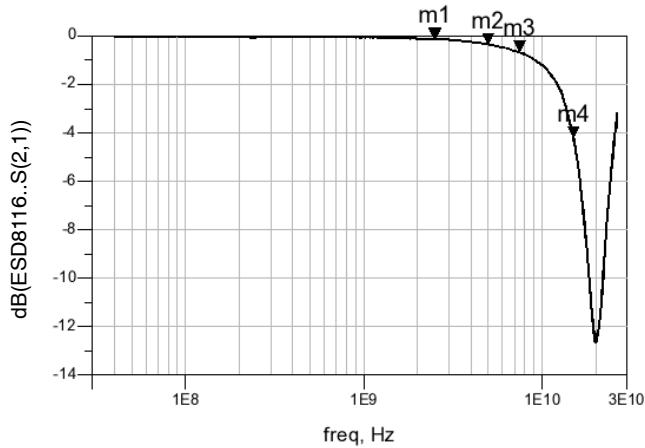


Figure 12. RF Insertion Loss

TABLE 1. RF Insertion Loss: Application Description

Interface	Data Rate (Gb/s)	Fundamental Frequency (GHz)	3rd Harmonic Frequency (GHz)	ESD8116 Insertion Loss (dB)
USB 3.0	5.0	2.5 (m1)	7.5 (m3)	m1 = 0.128 m2 = 0.155 m3 = 0.352 m4 = 4.194
USB 3.1	10	5.0 (m2)	15 (m4)	

## ESD8116

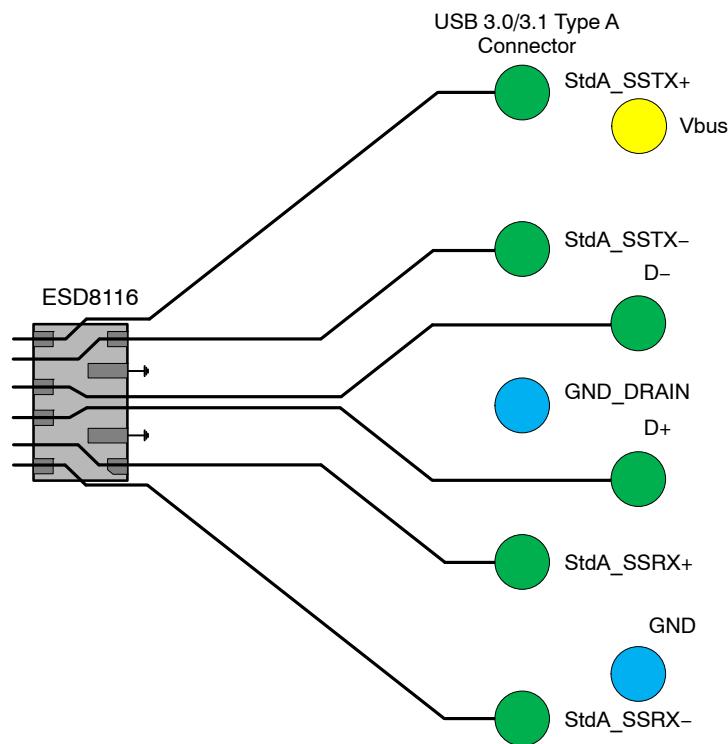
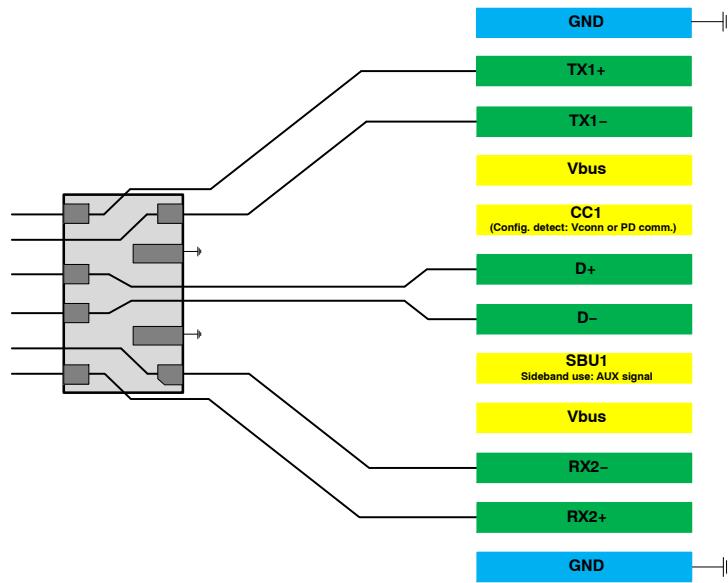


Figure 13. USB 3.0/3.1 Type-A Layout Diagram

# ESD8116

## Type-C Hybrid Top Mount Connector Top Layer



## Type-C Hybrid Top Mount Connector Bottom Layer

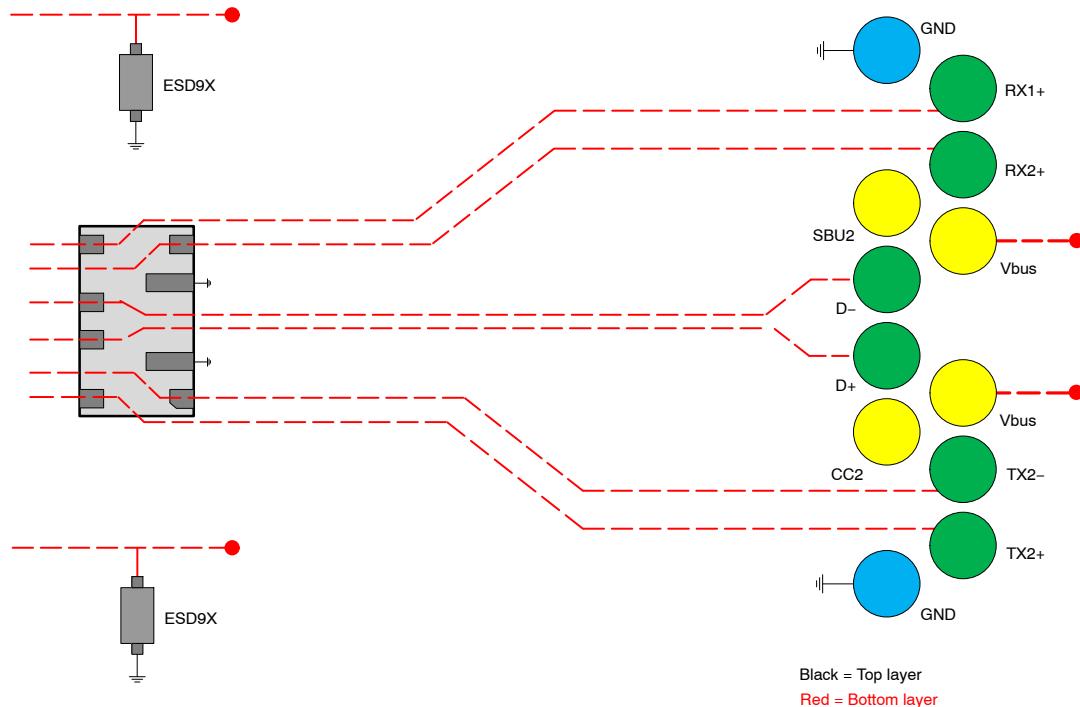


Figure 14. USB 3.1 Type-C Layout Diagram

### PCB Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

- Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.
  - ◆ In USB 3.0/3.1 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes.

- Make sure to use differential design methodology and impedance matching of all high speed signal traces.
  - ◆ Use curved traces when possible to avoid unwanted reflections.
  - ◆ Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.
  - ◆ Place grounds between high speed pairs and keep as much distance between pairs as possible to reduce crosstalk.

## ESD Protection Device Technology

ON Semiconductor's portfolio contains three main technologies for low capacitance ESD protection device which are highlighted below and in Figure 15.

- ESD7000 series: Zener diode based technology. This technology has a higher breakdown voltage (VBR) limiting it to protecting chipsets with larger geometries.
- ESD8000 series: Silicon controlled rectifier (SCR) type technology. The key advantage for this technology is a low holding voltage (VH) which produces a deeper snapback that results in lower voltage over high

currents as shown in the TLP results in Figure 16. This technology provides optimized protection for chipsets with small geometries against thermal failures resulting in chipset damage (also known as "hard failures").

- ESD8100 series: Low voltage punch through (LVPT) type technology. The key advantage for this technology is a very low turn-on voltage as shown in Figure 17. This technology provides optimized protection for chipsets with small geometries against recoverable failures due to voltage peaks (also known as "soft failures").

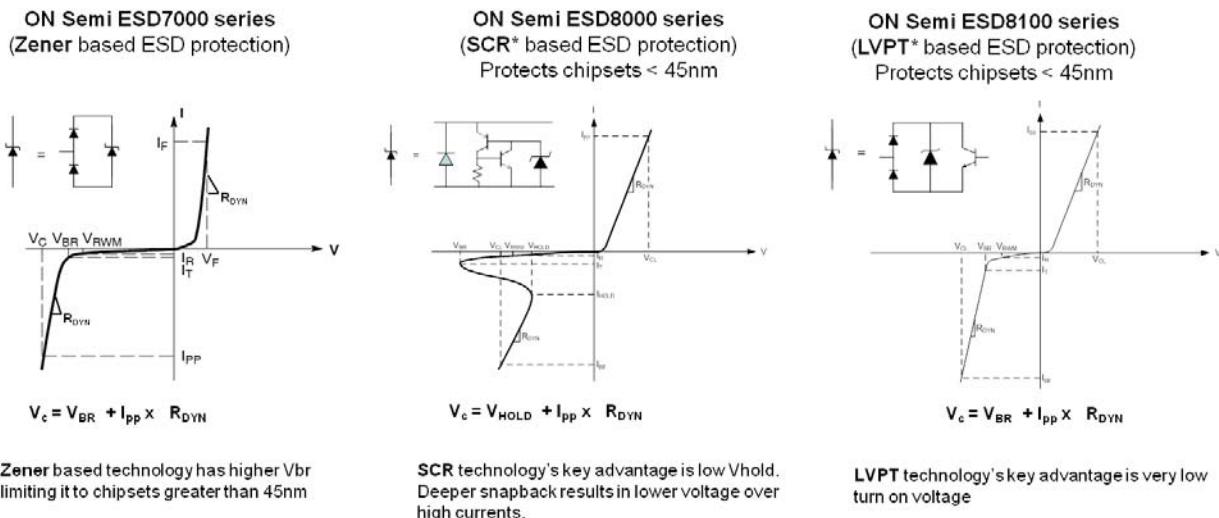


Figure 15. ON Semiconductor's Low-cap ESD Technology Portfolio

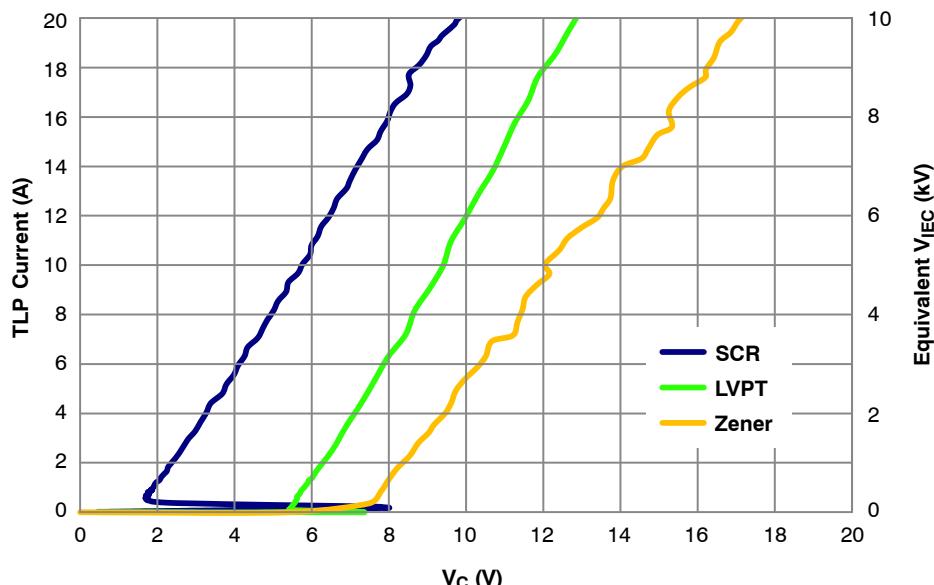


Figure 16. High Current, TLP, IV Characteristic of Each Technology

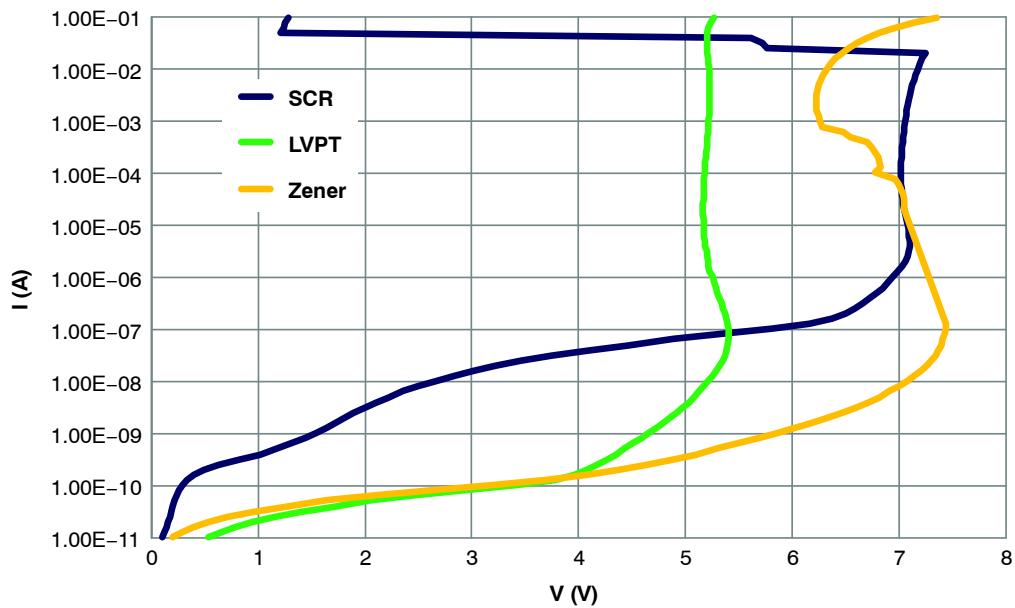
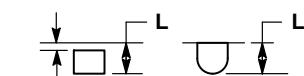
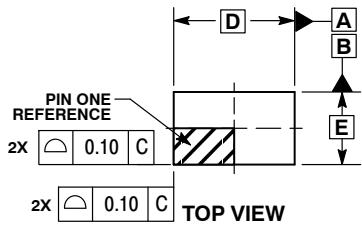


Figure 17. Low Current, DC, IV Characteristic of Each Technology

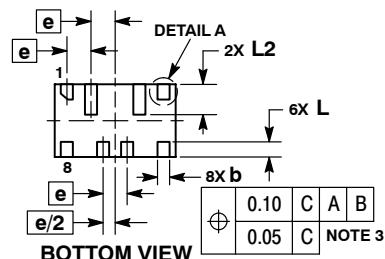
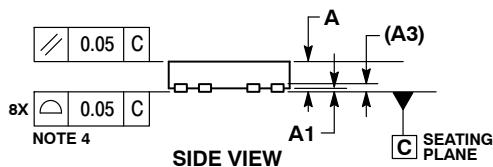
## PACKAGE DIMENSIONS

**UDFN8 2.0x1.2, 0.4P  
CASE 517CX  
ISSUE 0**



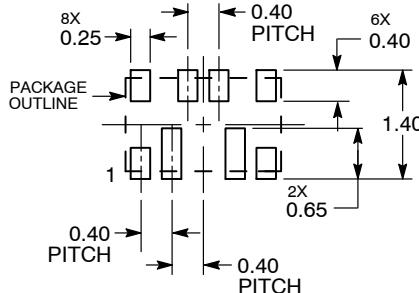
## **DETAIL A**

### **ALTERNATE TERMINAL CONSTRUCTIONS**



SHEET METAL FROM TIN		
DIM	MILLIMETERS	
	MIN	MAX
<b>A</b>	0.45	0.55
<b>A1</b>	0.00	0.05
<b>A3</b>	0.13	REF
<b>b</b>	0.15	0.25
<b>D</b>	2.00	BSC
<b>E</b>	1.20	BSC
<b>e</b>	0.40	BSC
<b>L</b>	0.15	0.35
<b>L1</b>	---	0.10
<b>L2</b>	0.40	0.60

## RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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