Design Example Report

Title	**18 W Automotive Power Supply with Planar Transformer for 800 V Systems Using InnoSwitch™3-AQ INN3949FQ**
Specification	100 VDC – 1000 VDC Input; 12.0 V / 1.5 A Output; 36 W (12 V, 3 A) Peak Output Power 30 VDC Start-up and Operation (7 W Output Power)
Application	Traction Inverter Gate-Driver Power Supply or Emergency Power Supply
Author	Automotive Systems Engineering Department
Document Number	DER-1039Q
Date	January 14, 2025
Revision	A

Summary and Features

- Ultra-compact design for 800 VDC automotive BEV applications
- Low component count (only 51 electrical components)
- Uses new InSOP28 (F) package which provides >5 mm Drain to Source pin spacing
- Wide-range start-up and operating voltage from <100 VDC to 1000 VDC[1]
- Planar transformer with reinforced isolation at 1000 V and complies with partial discharge (PD) and Hi-Pot requirements (IEC-60664-1 and IEC-60664-4)
- ≥80% full load efficiency across the input voltage range
- Accurate secondary-side regulation without optocouplers
- Provides continuous 18 W output from -40 °C to 85 °C[2]
- 36 W peak power for at least one minute at 85 °C[2]
- Comprehensive fault protection, including output current limit and short-circuit
- Uses automotive-qualified AEC-Q surface-mount (SMD) components[3]
- Low profile, only 12.5 mm high

[1] Derated power below 100 VDC input.
[2] Derated power beyond 85 °C up to 105 °C.
[3] Excluding customized transformer.

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

Table of Contents

Disclaimer:

The statements, technical information and recommendations contained herein are believed to be accurate as of the date hereof. Parameters, numbers, values, and other technical data included in the technical information were calculated and determined, to our best knowledge, to be in accordance with the relevant technical norms (if any). They may be based on assumptions or operational conditions that do not necessarily apply in general. We exclude any representation or warranty, express or implied, in relation to the accuracy or completeness of the statements, technical information and recommendations contained herein.

No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations, or opinions communicated and any liability for any direct, indirect, or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

1 Introduction

This engineering report describes an 18 W single-output automotive power supply for electric vehicles with an 800 V battery system. The design supports an ultra-wide input range of 100 VDC to 1000 VDC and uses the 1700 V rated INN3949FQ from the InnoSwitch3-AQ family of ICs in an isolated flyback configuration.

The design uses a planar transformer with reinforced isolation between the primary (high-voltage input) and secondary (low-voltage output) sides that complies with partial discharge (PD) and Hi-Pot test requirements. The planar transformer provides a low-profile design, ideal for applications with strict height constraints. It also offers low assembly cost and excellent transformer parameter repeatability compared to conventional wirewound transformers.

This document contains the power supply specification, schematic, printed circuit board (PCB) layout, bill of materials (BOM), details of the magnetics, and performance data.

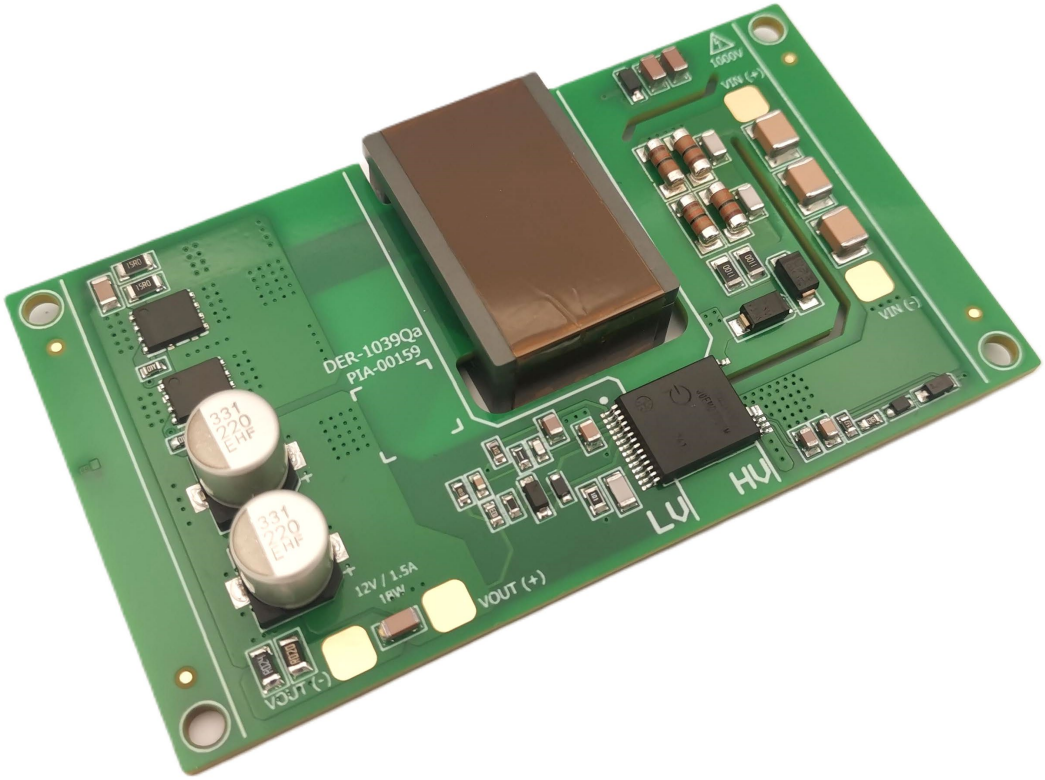


Figure 1 – Populated Circuit Board, Oblique View of Top Side.

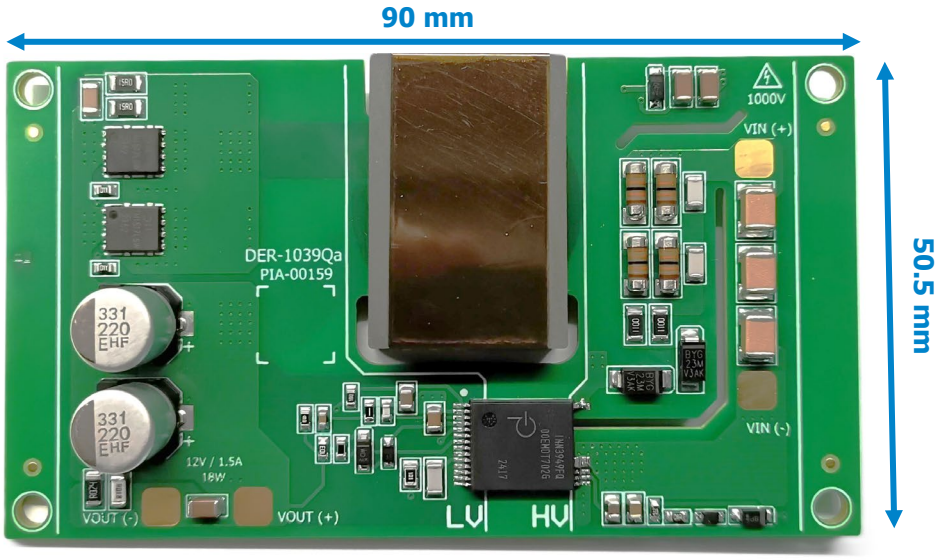


Figure 2 – Populated Circuit Board, Top View.

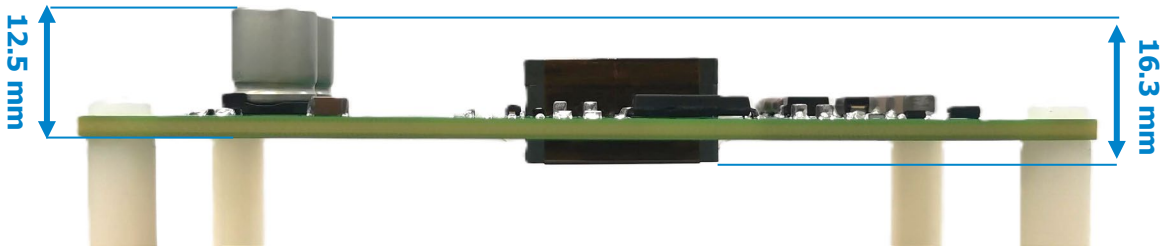


Figure 3 – Populated Circuit Board, Side View.

The design can deliver the rated 18 W output power continuously at 85 °C ambient from 100 VDC to 1000 VDC input, with derated output power beyond 85 °C up to 105 °C ambient. The design can also deliver 36 W peak power for at least 1 minute and 24 W for at least 5 minutes at 85 °C ambient from 100 VDC to 1000 VDC input. Start-up at 30 VDC is also guaranteed with loads up to 7 W. The 12 V output configuration allows the design to serve as either a traction inverter gate driver power source or as emergency power supply.

The InnoSwitch3-AQ IC maintains regulation by directly sensing the output voltage and providing fast, accurate feedback to the primary-side via FluxLink™ magneto-inductive coupling. The secondary-side controller also simplifies the implementation of synchronous rectification, improving overall efficiency (compared to diode rectification) - saving space by eliminating heatsinks.

2 Design Specification

The following tables represent the minimum acceptable performance of the design. Actual performance is listed in the results section.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC-Link Input Voltage Referenced to HV-	**HV**	100	800	1000	VDC
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	V_{OUT}	11.4	12	12.6	VDC
Output Voltage Load and Line Regulation	V_{REG}	-5		+5	%
Ripple Voltage Measured on Board	V_{RIPPLE}			400	mV
Output Current Parameters					
Output Current	I_{OUT}		1.5	3[4]	A
Output Power Parameters[5]					
Continuous Output Power at 100 VDC – 1000 VDC Input	P_{OUT}		18		W
Peak Output Power at 100 VDC – 1000 VDC Input for 1 minute				36	
Peak Output Power at 100 VDC – 1000 VDC Input for 5 minutes				24	
Output Overshoot and Undershoot During Dynamic Load Condition					
0% - 50% - 0% Transient Load	ΔV_{OUT}	-5		+5	%
50% - 100% - 50% Transient Load					
10% - 90% - 10% Transient Load					
Operating Parameters					
Operating Switching Frequency	f_{SW}		40	65.2	kHz

Table 1 – Electrical Specifications.

[4] Maximum peak output current at peak output power.
[5] From -40 °C to 85 °C ambient. For maximum output power capability at 105 °C, see Section 13.

2.2 Isolation

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3949FQ	BV_{DSS}			1700	V
System Voltage	V_{SYSTEM}			1400	V
Working Voltage	$V_{WORKING}$			1000	V
Pollution Degree	PD			2	
CTI for FR4	CTI	175			
Rated Impulse Voltage	$V_{IMPULSE}$			2.50	kV
Altitude Correction Factor for h_a	C_{ha}			1.59	
Technical Cleanliness				1.0	mm
Basic Clearance Distance Requirement	CLR_{BASIC}	3.4			mm
Reinforced Clearance Distance Requirement	$CLR_{REINFORCED}$	5.8			mm
Basic Creepage Distance Requirement for PCB	$CPG_{BASIC(PCB)}$	6.0			mm
Reinforced Creepage Distance Requirement for PCB	$CPG_{REINFORCED(PCB)}$	11.0			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60 s	V_{ISO}	4000			V_{RMS}
Partial Discharge Test Voltage	V_{PD_TEST}	2100			V_{PK}

Table 2 – Isolation[6].

2.3 Environmental Specification

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	Ta	-40		105[7]	°C
Altitude of Operation	h_a			5500	m

Table 3 – Environmental Specifications.

[6] Clearance and creepage distances were calculated according to IEC 60664-1 and IEC 60664-4.
[7] Derated power beyond 85 °C up to 105 °C.

3 Schematic[8]

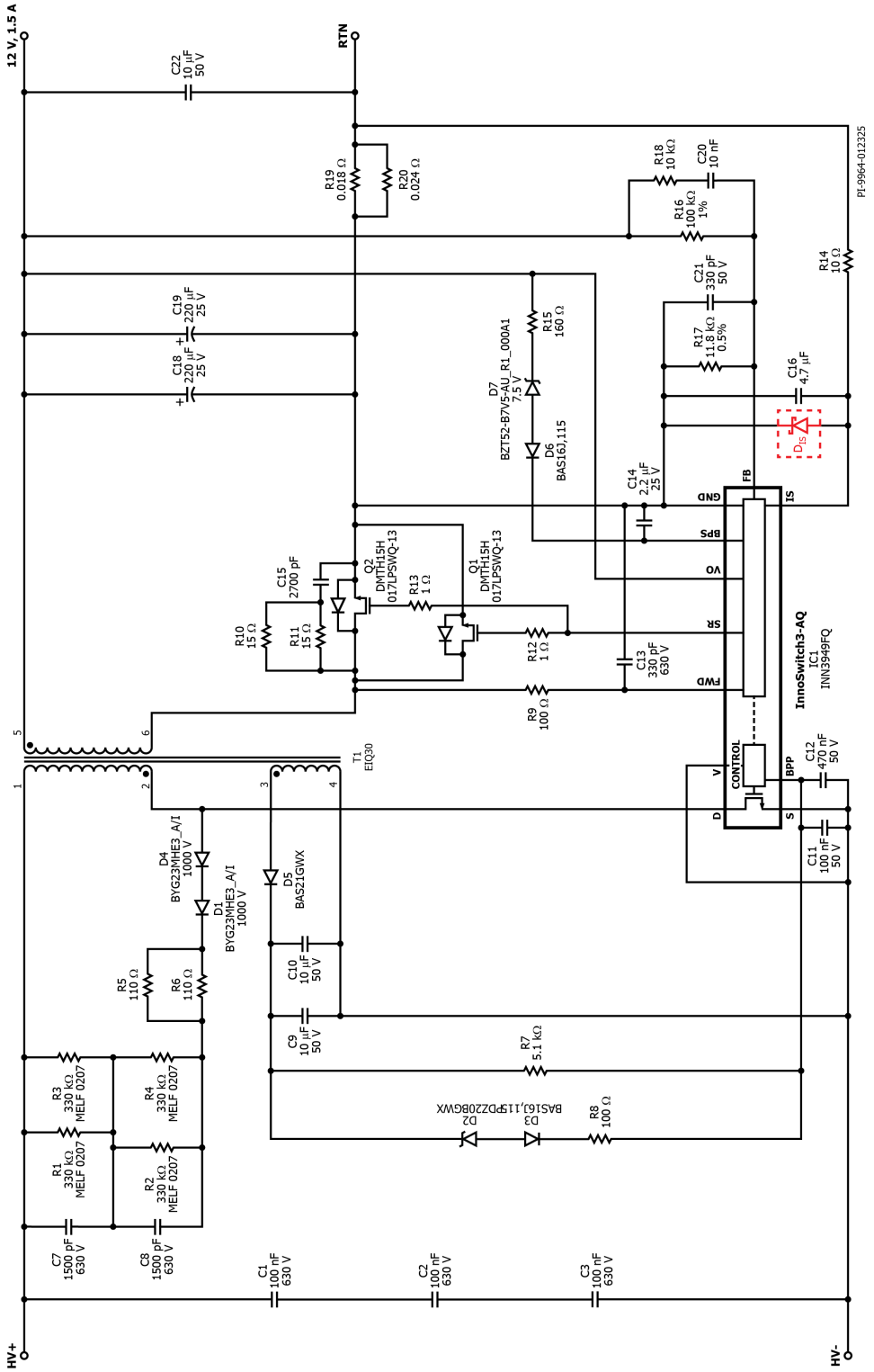


Figure 4 – DER-1039Q Schematic.

[8] D_{IS} (enclosed within the dashed box) is not included in the DER-1039Q board but is recommended for IS pin protection to clamp maximum pin voltage transient when output is short circuited.

4 Circuit Description

4.1 Input Filter

The automotive inverter environment is harsh and characterized by high dv/dt and di/dt from the switching action of the power modules. These transient events can create high levels of electrical noise that can interfere with the power supply's operation. The bypass capacitors C1 to C3 reduce the noise entering the power supply and prevent it from affecting the overall performance of the design. These capacitors also minimize the primary-side current loop. The capacitors are selected so as not to experience more than 65% of their voltage rating. They are also chosen with a pin geometry to enable pad spacing that meets creepage and clearance requirements.

4.2 High-Voltage Circuit

The power supply uses a flyback converter topology that provides an isolated low-voltage output from the high-voltage input. The primary winding of the flyback planar transformer T1 is connected between the high-voltage DC input and the drain pin of the 1700 V SiC power switch integrated into the InnoSwitch3-AQ IC (IC1).

An R2CD-type snubber circuit is placed across the primary winding to limit the drain-source voltage peak during turn-off. Two super-fast diodes (D1 and D4) were placed in series to meet creepage and clearance requirements. This also ensures that the reverse voltage across the diodes does not exceed 70% of their maximum rating. Capacitors C7 and C8 store the energy from the leakage inductance of transformer T1. The capacitor values were selected to minimize the voltage ripple across the snubber resistor network and maintain near-constant power dissipation through the switching cycle. Resistors R1 to R4 dissipate the energy stored by the snubber capacitors. The resistor values were selected such that the snubber voltage will not exceed 80% of their maximum rated voltage and to ensure that they will dissipate less than 50% of their rated power.

The auxiliary winding of transformer T1 provides power to the primary-side during normal operation. This improves efficiency and reduces the heating of the InnoSwitch3-AQ IC. The auxiliary winding output is rectified and filtered by diode D5 and capacitors C9 and C10. The InnoSwitch3-AQ IC is self-starting, using an internal high-voltage current source to charge the BPP capacitors, C12 and C11. Current is injected into the BPP capacitors through resistor R7. Diodes D2, D3, and resistor R8 serve as a primary-sensed output overvoltage protection (primary OVP) circuit, which injects current to the BPP pin of InnoSwitch3-AQ IC during output overvoltage events, driving the IC to enter auto-restart (AR) as long as the fault is present.

In this design, line undervoltage (UV) and overvoltage (OV) features were disabled by shorting the V pin to the SOURCE pin. This allows the design to operate at inputs as low as 30 VDC.

4.3 Low-Voltage Circuit

The secondary-side of the InnoSwitch3-AQ IC provides output voltage sensing, output current sensing, and gate drive for the synchronous rectification MOSFET (SR FET). SR FETs Q1 and Q2 rectify the voltage across the secondary winding of the transformer T1, then filtered by output capacitors C18 and C19. An RC snubber formed by resistors R10 and R11 and capacitor C15 damps high-frequency ringing across the SR FET.

The secondary-side controller inside the InnoSwitch3-AQ IC controls the switching of the SR FETs. Timing is based on the negative edge voltage transition sensed by the FWD pin via resistor R9. Capacitor C13 and resistor R9 form a low-pass filter that reduces voltage spikes seen by the FWD pin and ensures that the maximum rating of 150 V is not exceeded.

In continuous conduction mode (CCM) operation, the SR MOSFET is turned off just before the secondary-side controller requests a new switching cycle from the primary. In discontinuous conduction mode (DCM), the SR MOSFET is turned off when the voltage across it rises above $V_{SR(TH)}$ (~-3.3 mV). Secondary-side control of the primary-side switch prevents cross-conduction, ensuring reliable SR operation.

The secondary-side of the InnoSwitch3-AQ IC is powered by either the secondary winding forward voltage (through R9 and the FWD pin) or the output voltage (through the VOUT pin). The BPS capacitor C14 is charged via an internal regulator in both cases.

Diodes D6, D7, and resistor R15 form the secondary-side output overvoltage protection circuit. During output overvoltage events, the diodes turn on, and current is injected into the BPS pin of InnoSwitch3-AQ IC, triggering AR. This network protects for faults on the secondary when the secondary controller is functional. When the secondary controller is not functional, the primary side BPP pin-based output OV function is recommended.

The InnoSwitch3-AQ IC's FB pin has an internal 1.265 V reference. Resistors R16 and R17 form the voltage divider feedback network. Capacitor C21 provides decoupling of high-frequency noise. C20 and R18 increase the ripple content of the FB pin for improved transient response and lower output ripple.

The parallel combination of output current sense resistors R19 and R20 sets the output current limit. The voltage across R19 and R20 is compared to an internal threshold of around 35 mV. Once reached, secondary requests will be inhibited causing output voltage to drop. The IC will enter auto-restart (AR) operation when the output voltage falls 10% below regulation during CC mode and recovers when the load current is reduced below the CC limit.

5 PCB Layout

Layers: Eight (8)
Board Material: FR4
Board Thickness: 2 mm
Copper Weight: 1 oz

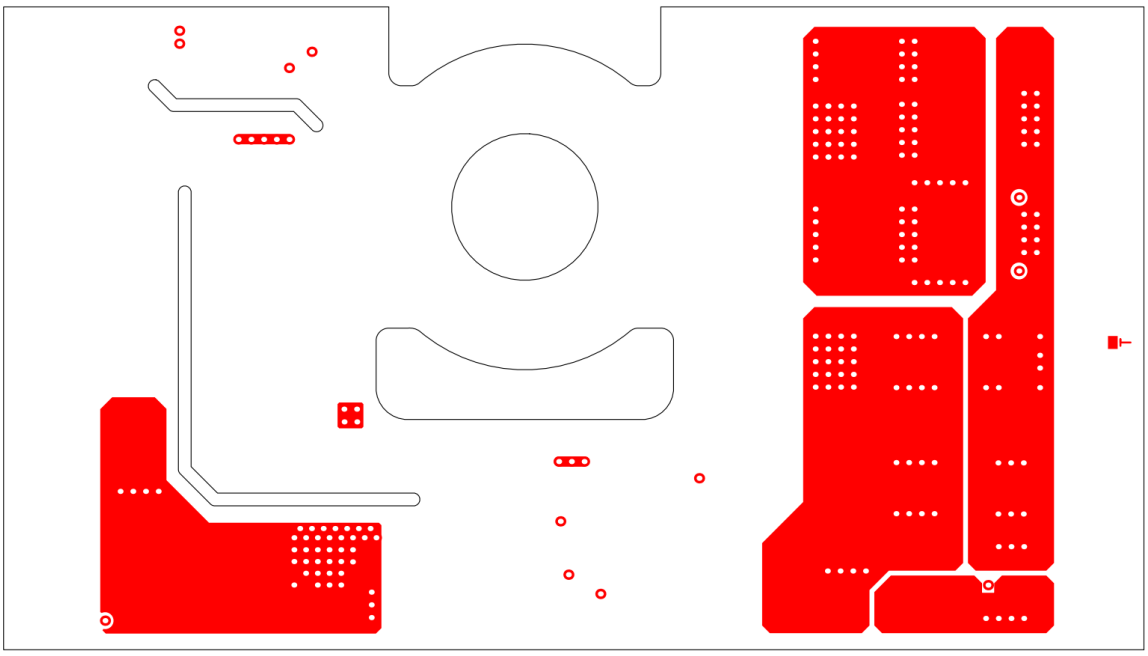


Figure 5 – DER-1039Q Top Layer PCB Layout.

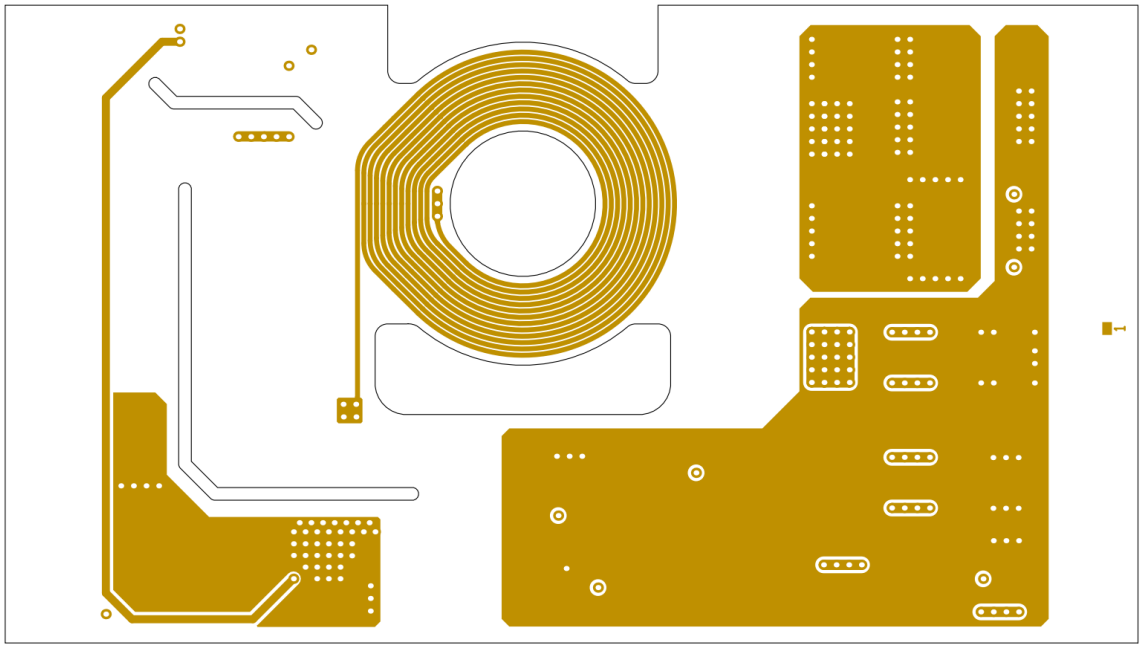


Figure 6 – DER-1039Q Mid-Layer 1 PCB Layout.

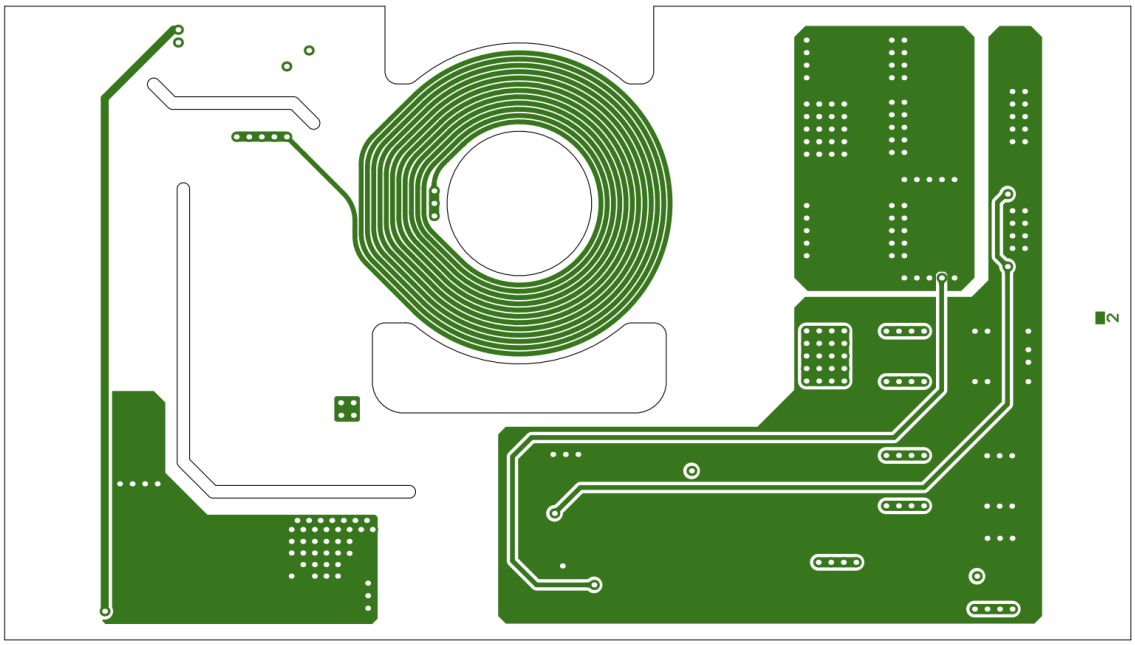


Figure 7 – DER-1039Q Mid-Layer 2 PCB Layout

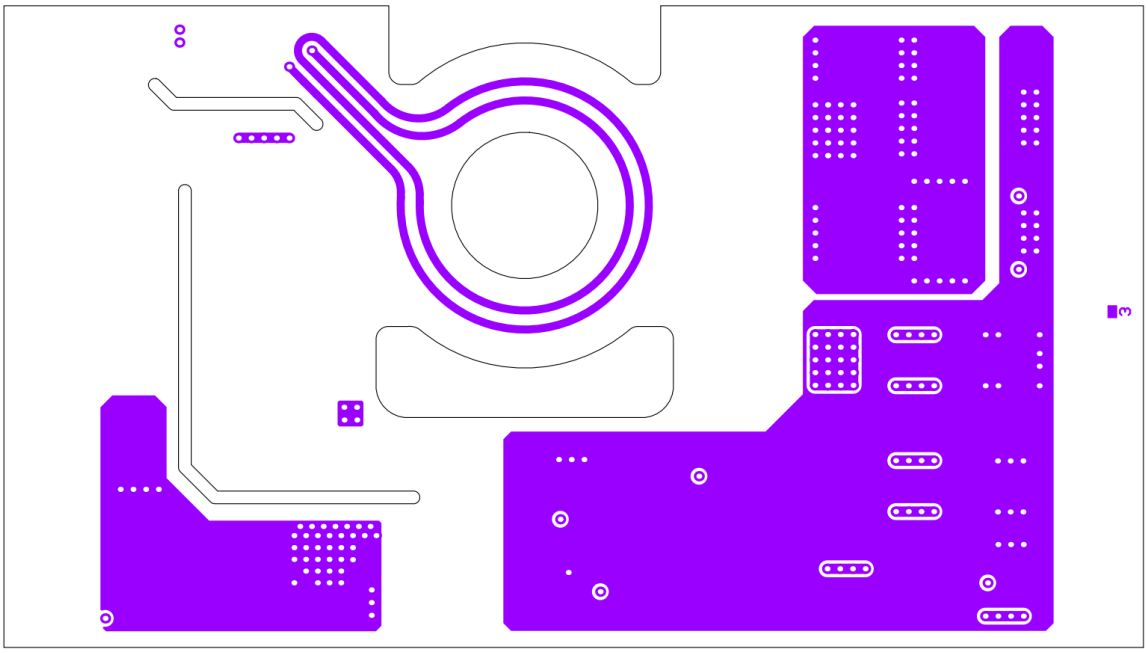


Figure 8 – DER-1039Q Mid-Layer 3 PCB Layout.

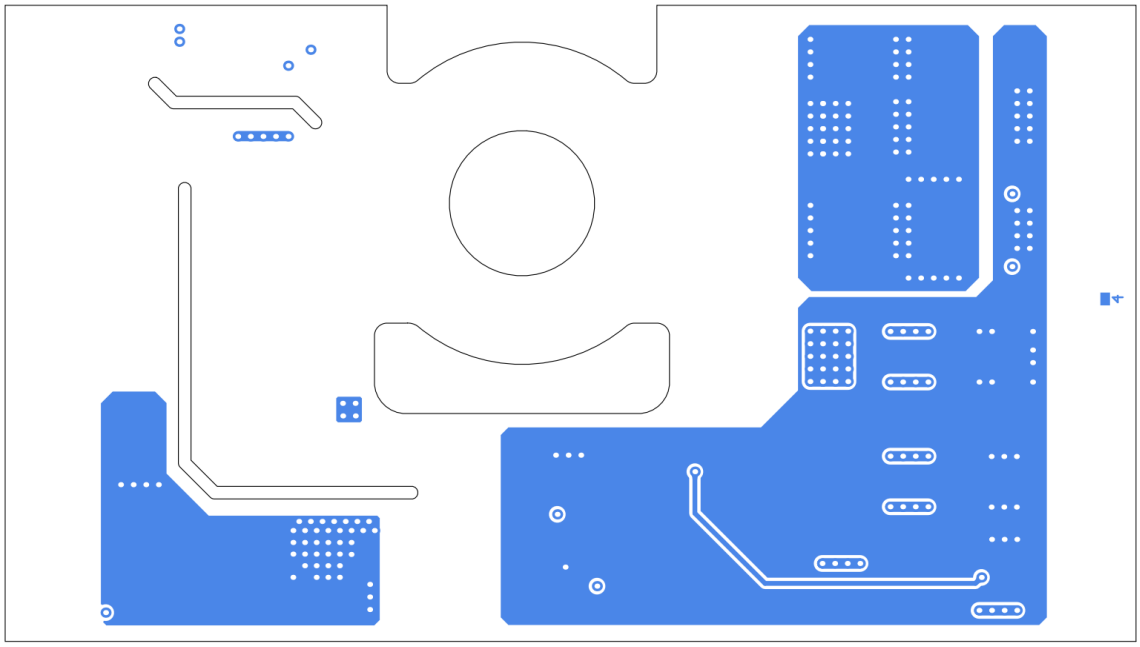


Figure 9 – DER-1039Q Mid-Layer 4 PCB Layout.

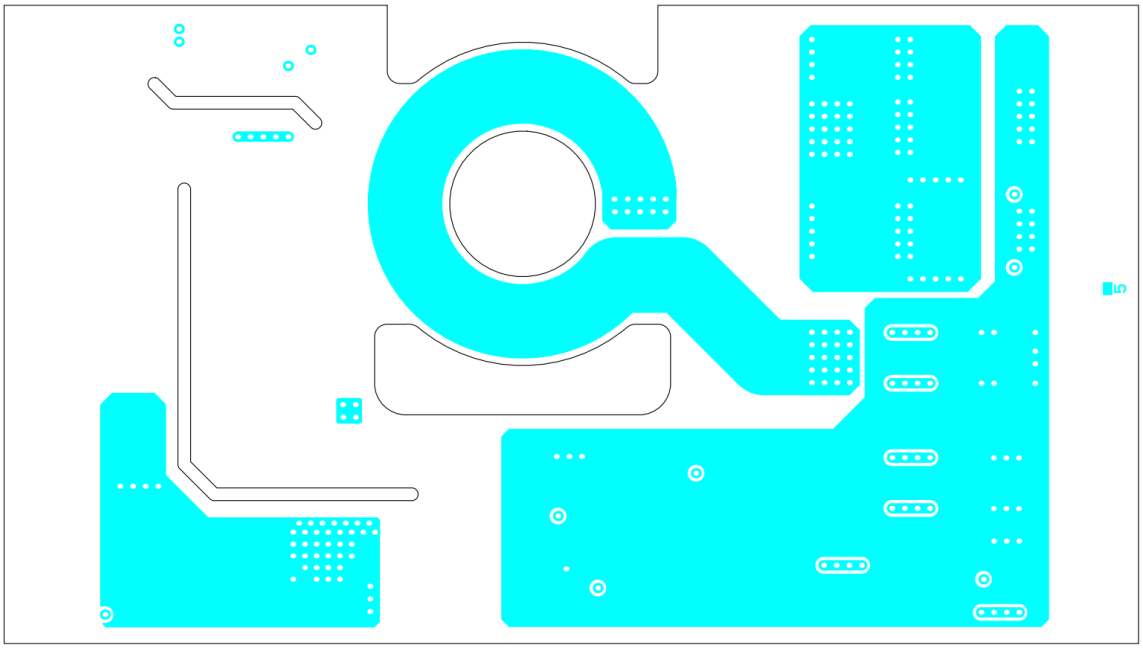


Figure 10 – DER-1039Q Mid-Layer 5 PCB Layout.

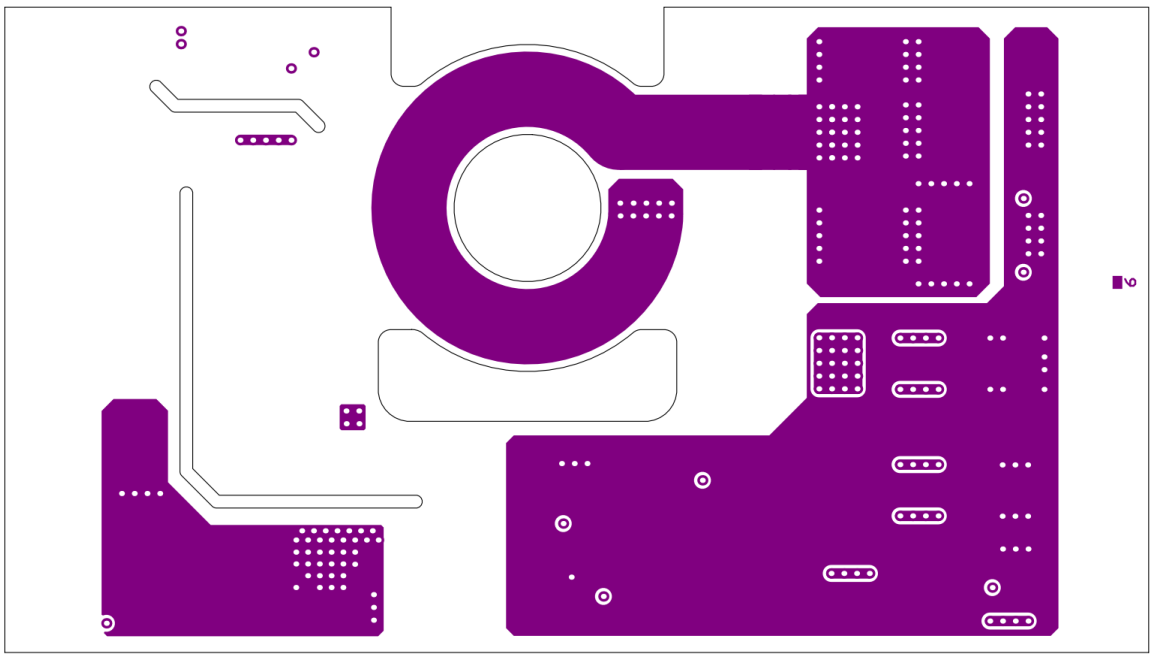


Figure 11 – DER-1039Q Mid-Layer 6 PCB Layout.

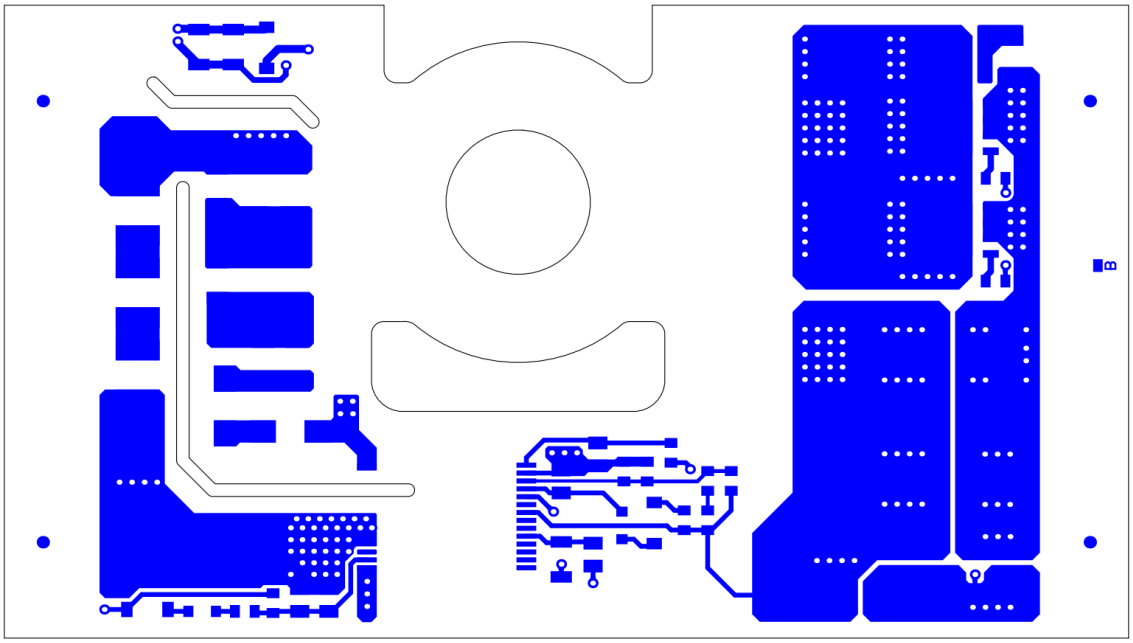


Figure 12 – DER-1039Q Bottom Layer PCB Layout.

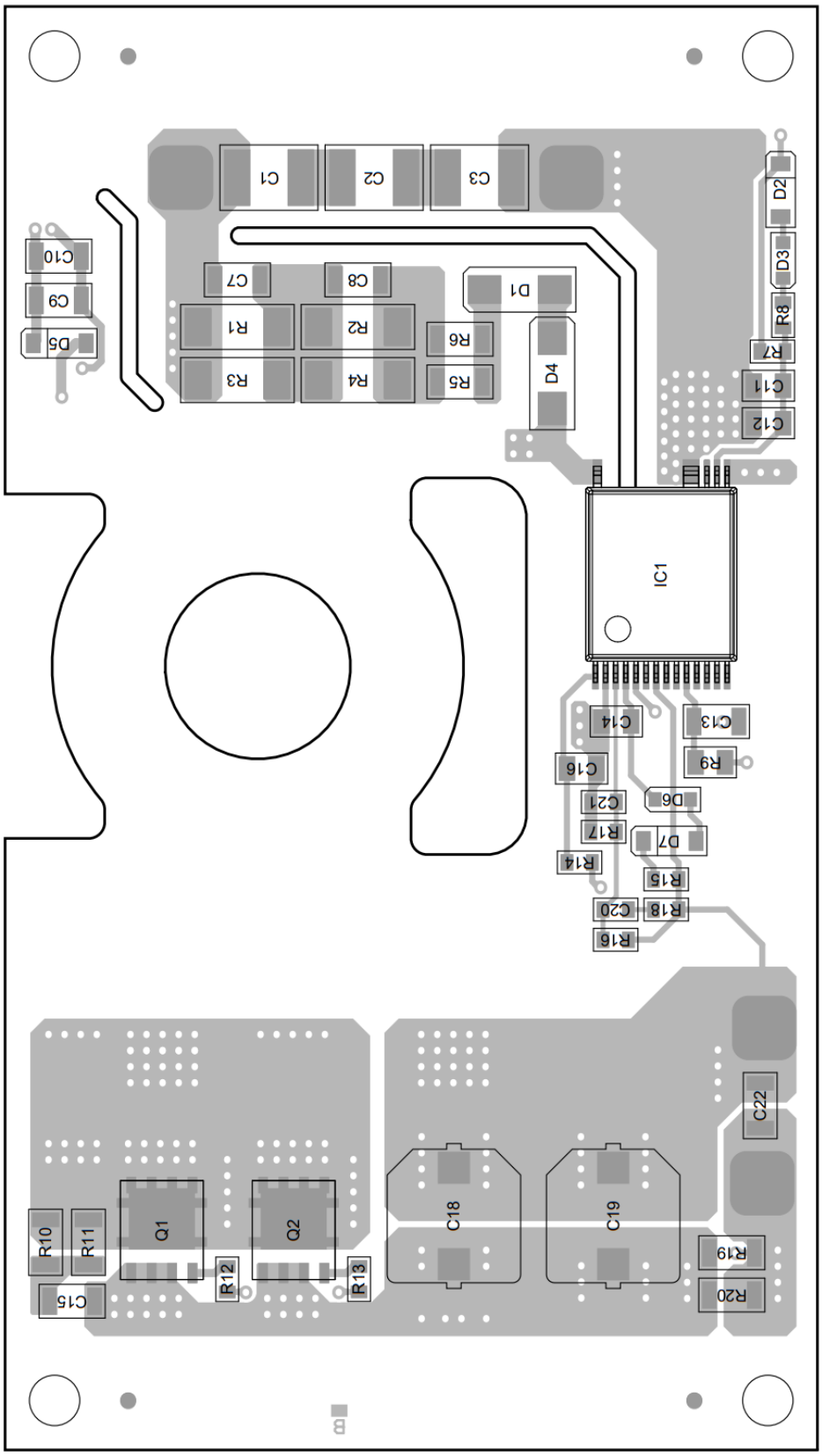


Figure 13 – DER-1039Q PCB Assembly.

6 Bill of Materials

Item	Qty	Designator	Description	MFR Part Number	Manufacturer
1	3	C1, C2, C3	Multilayer Ceramic Capacitors MLCC - SMD/SMT 100n X7R 630 V 10% 1812 AEC-Q200	CGA8N4X7R2J104K230KE	TDK
2	2	C7, C8	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1500p C0G 630 V 5% 1206 AEC-Q200	CGA5H4C0G2J152J115AA	TDK
3	3	C9, C10, C22	Multilayer Ceramic Capacitors MLCC - SMD/SMT 10u X7R 50 V 10% 1206 AEC-Q200	CGA5L1X7R1H106K160AE	TDK
4	1	C11	Multilayer Ceramic Capacitors MLCC - SMD/SMT 100n X7R 50 V 20% 805 AEC-Q200	CGA4J2X7R1H104M125AE	TDK
5	1	C12	Multilayer Ceramic Capacitors MLCC - SMD/SMT 470n X7R 50 V 10% 805 AEC-Q200	CGA4J3X7R1H474K125AE	TDK
6	1	C13	Multilayer Ceramic Capacitors MLCC - SMD/SMT 330p C0G 630 V 5% 1206 AEC-Q200	CGA5C4C0G2J331J060AA	TDK
7	1	C14	Multilayer Ceramic Capacitors MLCC - SMD/SMT 2u2 X7R 25 V 10% 805 AEC-Q200	CGA4J3X7R1E225K125AE	TDK
8	1	C15	Multilayer Ceramic Capacitors MLCC - SMD/SMT 2700p C0G 630 V 2% 1206 AEC-Q200	C1206C272GBGACAUTO	KEMET
9	1	C16	Multilayer Ceramic Capacitors MLCC - SMD/SMT 4u7 X7R 25 V 20% 805 AEC-Q200	CGA4J1X7R1E475M125AC	TDK
10	2	C18, C19	Polymer Aluminum Capacitor 220u 25 V 20% AEC-Q200	HHXF250ARA221MHA0G	Chemi-Con
11	1	C20	Multilayer Ceramic Capacitors MLCC - SMD/SMT 10n X7R 50 V 20% 603 AEC-Q200	C0603C103M5RACAUTO	KEMET
12	1	C21	Multilayer Ceramic Capacitors MLCC - SMD/SMT 330p C0G 50 V 5% 603 AEC-Q200	C0603C331J5GACAUTO	KEMET
13	2	D1, D4	Diode 1000 V 1.5 A Surface Mount DO-214AC AEC-Q101	BYG23MHE3_A/I	Vishay
14	1	D2	Zener Diode 20 V 365 mW ±2.18% Surface Mount SOD-123 AEC-Q101	PDZ20BGWX	Nexperia
15	2	D3, D6	Diode 100 V 250 mA Surface Mount SOD-323F AEC-Q101	BAS16J,115	Nexperia
16	1	D5	Diode 200 V 225 mA Surface Mount SOD-123 AEC-Q101	BAS21GWX	Nexperia
17	1	D7	Zener Diode 7.5 V 410 mW ±2% Surface Mount SOD-123 AEC-Q101	BZT52-B7V5-AU_R1_000A1	Panjit International Inc.
18	1	IC1	CV/CC QR Flyback Switcher IC with Integrated 1700 V Switch and FluxLink Feedback for Automotive Applications	INN3949FQ	Power Integrations
19	2	Q1, Q2	N-Channel 150 V 8 A (Ta), 50 A (Tc) 1.5 W (Ta), 107 W (Tc) Surface Mount, Wettable Flank PowerDI5060-8 (Type UX) AEC-Q101	DMTH15H017LPSWQ-13	Diodes
20	4	R1, R2, R3, R4	330 kOhms ±1% 1 W Chip Resistor MELF, 0207 Anti-Sulfur, Automotive AEC-Q200 Thin Film	MMB02070C3303FB200	Vishay
21	2	R5, R6	110 Ohms ±1% 0.25 W, 1/4 W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200 Thick Film	RMCF1206FT110R	Stackpole Electronics Inc
22	1	R7	5.1 kOhms ±5% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC0603JR-075K1L	YAGEO
23	1	R8	100 Ohms ±1% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC0603FR-13100RL	YAGEO
24	1	R9	100 Ohms ±5% 0.125 W, 1/8 W Chip Resistor 0805 (2012 Metric) Automotive AEC-Q200 Thick Film	ERJ-6GEYJ101V	Panasonic
25	2	R10, R11	15 Ohms ±1% 0.25 W, 1/4 W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC1206FR-0715RL	YAGEO

26	2	R12, R13	1 Ohms ±1% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC0603FR-071RL	YAGEO
27	1	R14	10 Ohms ±1% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	RMCF0603FT10R0	Stackpole Electronics Inc
28	1	R15	160 Ohms ±1% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	ERJ-3EKF1600V	Panasonic
29	1	R16	100 kOhms ±1% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	RMCF0603FT100K	Stackpole Electronics Inc
30	1	R17	11.8 kOhms ±0.5% 0.2 W, 1/5 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Pulse Withstanding Thick Film	ERJ-PB3D1182V	Panasonic
31	1	R18	10 kOhms ±5% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC0603JR-0710KL	YAGEO
32	1	R19	18 mOhms ±1% 0.5W, 1/2W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200, Current Sense Thick Film	UCR18EVHFSR018	Rohm Semiconductor
33	1	R20	24 mOhms ±1% 0.25 W, 1/4 W Chip Resistor 1206 (3216 Metric) Current Sense Thick Film	RL1206FR-070R024L	YAGEO
34	1	T1	18 W Power Transformer	ElQ30	Power Integrations
35	1	T1-Core	3C96 Ferrite Core	EQ30 – 3C96	Ferroxcube
36	1	T1-Core	3C96 Ferrite Core	PLT30/20/3 – 3C96	Ferroxcube
37	1	Z2	Printed Circuit Board	PIA-00159	Power Integrations

Table 4 – DER-1039Q Bill of Materials[9].

[9] All components are AEC-Q qualified except the transformer.

7 Transformer Specification (T1)

7.1 Electrical Diagram

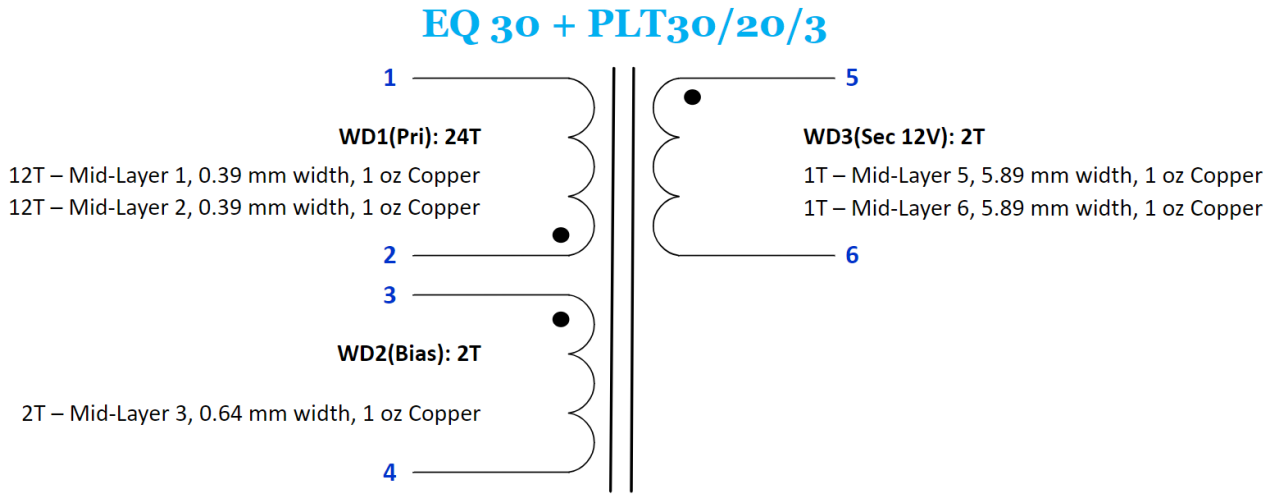


Figure 14 – Transformer Electrical Diagram.

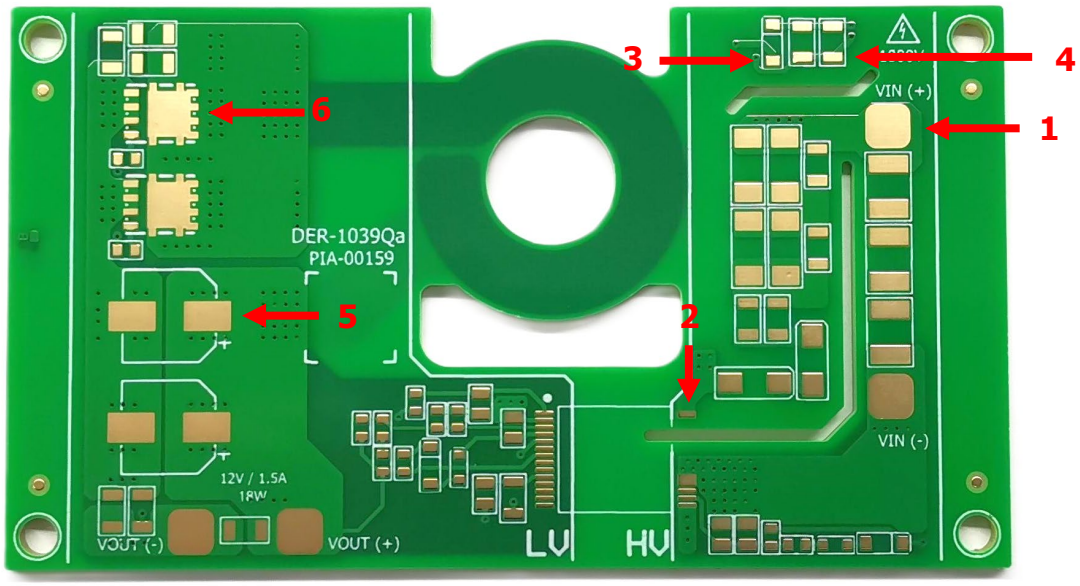


Figure 15 – DER-1039Q Planar Transformer Test Nodes.

7.2 Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side		18	36[10]	W
Input voltage VDC	Flyback topology	100	800	1000	VDC
Switching frequency			40	65.2	kHz
Duty cycle		2.6		42.9	%
Turns Ratio (N_P:N_S)			12		
Primary Winding Resistance ($R_{DC,PRI}$)	All windings open		2.2		Ω
Secondary Winding Resistance ($R_{DC,SEC}$)			13.7		mΩ
Coupling capacitance	Primary-side to secondary-side Measured at 1 V_{PK-PK}, 100 kHz frequency, between node 2 to node 6, with nodes 1 - 2 shorted and nodes 5 - 6 shorted at 25 °C		25		pF
Primary inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between node 1 to node 2, with all other windings open at 25 °C		450		µH
Part-to-part tolerance	Tolerance of Primary Inductance	-5.0		5.0	%
Primary leakage inductance	Measured between node 1 to node 2, with all other windings shorted.		18.2		µH

Table 5 – Transformer (T1) Electrical Specifications.

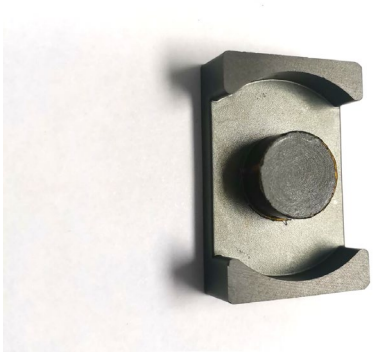
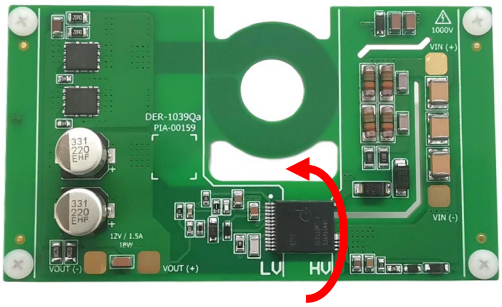
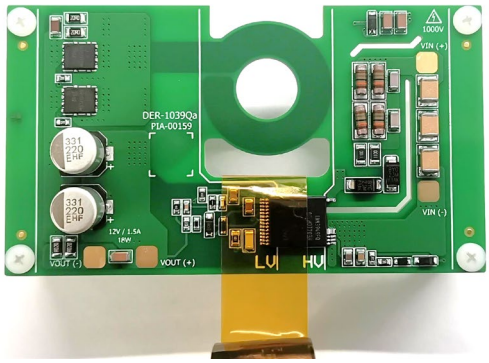
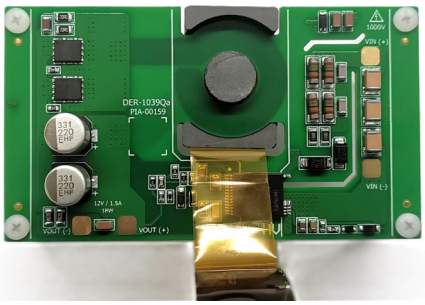
7.3 Material List

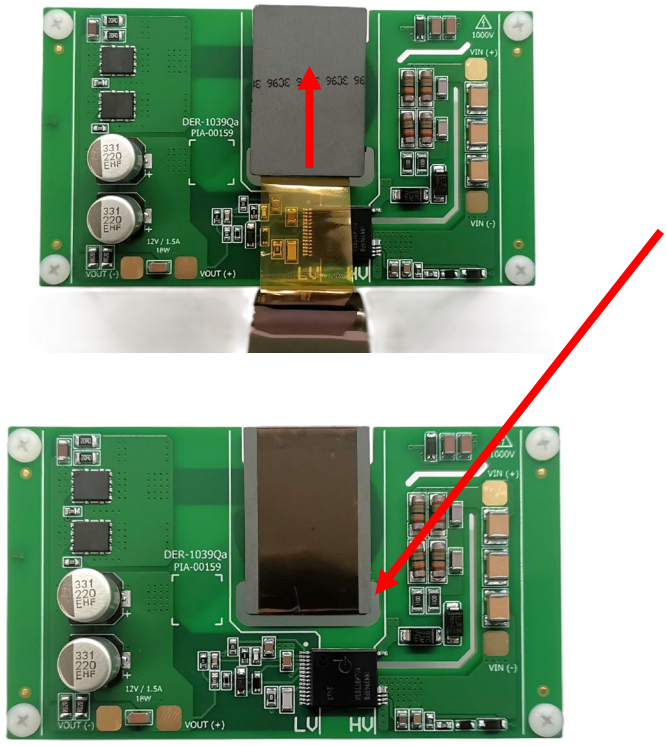
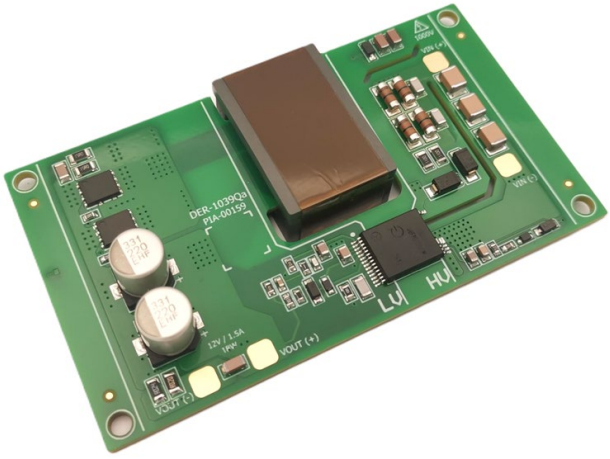
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Core: EQ30	1	PC	3C96 (or equivalent)	Ferroxcube
[2]	Core: PLT30/20/3	1	PC	3C96 (or equivalent)	Ferroxcube
[3]	3M Polyimide Film Tape 5413, width: 0.625 in (15.9 mm)		mm	3M 5413 0.625" X 36YD (or equivalent)	3M

Table 6 – Transformer (T1) Material List.

[10] Peak output power for 1 minute

7.4 Transformer Assembly Instructions

Core Preparation		Gap EQ core (Item [1]) to get 450 µH ± 5% of inductance between nodes 1 and 2.
Transformer Assembly	  	Insert tape (Item [3]) facing the sticky side into the lower slot of the planar transformer. Stick the tape on the table for support. Place the gapped EQ core (Item [1]) and PLT core (Item [2]) into the planar transformer slot.

		Hold the transformer core and tightly fasten it by applying one layer of tape (Item [3]). This slot is intended for the installation of an insulating spacer to maintain primary to secondary creepage and clearance requirements. This is to avoid making the PCB wider to accommodate the worst case horizontal position of the core relative to traces and components. The insulating spacer is not included in this report but is required for a production design unless the planar transformer is spaced an additional 5 mm and when the board width increases by the same amount.
Finishing		Fasten the core to the PCB using epoxy. The gapped section of the core should be positioned away from the PCB.

8 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3AQ_Flyback_022024; Rev.3.8; Copyright Power Integrations 2024	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VOUT	12.00		12.00	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	1000.00		1000.00	V	Input DC voltage 1
6	IOUT1	1.500		1.500	A	Output current 1
7	POUT1			18.00	W	Output power 1
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	**OPERATING CONDITION 2**					
12	VINDC2	800.00		800.00	V	Input DC voltage 2
13	IOUT2	1.500		1.500	A	Output current 2
14	POUT2			18.00	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
18	**OPERATING CONDITION 3**					
19	VINDC3	100.00		100.00	V	Input DC voltage 3
20	IOUT3	1.500		1.500	A	Output current 3
21	POUT3			18.00	W	Output power 3
22	EFFICIENCY3			0.85		Converter efficiency for output 3
23	Z_FACTOR3			0.50		Z-factor for output 3
69	**PRIMARY CONTROLLER SELECTION**					
70	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
71	VDRAIN_BREAKDOWN	1700		1700	V	Device breakdown voltage
72	DEVICE_GENERIC			INN39X9		Device selection
73	DEVICE_CODE	INN3949FQ		INN3949FQ		Device code
74	PDEVICE_MAX			70	W	Device maximum power capability
75	RDSON_25DEG			0.62	Ω	Primary switch on-time resistance at 25 °C
76	RDSON_125DEG			1.10	Ω	Primary switch on-time resistance at 125 °C
77	ILIMIT_MIN			1.767	A	Primary switch minimum current limit
78	ILIMIT_TYP			1.900	A	Primary switch typical current limit
79	ILIMIT_MAX			2.033	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			0.22	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			1174	V	Peak drain voltage on the primary switch during turn-off
85	**WORST CASE ELECTRICAL PARAMETERS**					
86	FSWITCHING_MAX	40000		40000	Hz	Maximum switching frequency at full load and minimum DC input voltage
87	VOR	144.0		144.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			4.020		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			DCM		Mode of operation
90	DUTYCYCLE			0.264		Primary switch duty cycle
91	TIME_ON_MIN			0.65	µs	Minimum primary switch on-time
92	TIME_ON_MAX			7.65	µs	Maximum primary switch on-time
93	TIME_OFF			18.52	µs	Primary switch off-time
94	LPRIMARY_MIN			427.3	µH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			449.8	µH	Typical primary magnetizing inductance
96	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			472.3	µH	Maximum primary magnetizing inductance

99	**PRIMARY CURRENT**					
100	IAVG_PRIMARY			0.196	A	Primary switch average current
101	IPEAK_PRIMARY			1.650	A	Primary switch peak current
102	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			1.650	A	Primary switch ripple current
104	IRMS_PRIMARY			0.465	A	Primary switch RMS current
108	**TRANSFORMER CONSTRUCTION PARAMETERS**					
109	**CORE SELECTION**					
110	CORE	EQ30		EQ30		Core selection
111	CORE NAME			EQ30-3C96		Core code
112	AE			108.0	mm^2	Core cross sectional area
113	LE			36.2	mm	Core magnetic path length
114	AL			6000	nH	Ungapped core effective inductance per turns squared
115	VE			3910	mm^3	Core volume
122	**PRIMARY WINDING**					
123	NPRIMARY			24		Primary winding number of turns
124	BPEAK			3791	Gauss	Peak flux density
125	BMAX			2944	Gauss	Maximum flux density
126	BAC			1472	Gauss	AC flux density (0.5 x Peak to Peak)
127	ALG			781	nH	Typical gapped core effective inductance per turns squared
128	LG			0.151	mm	Core gap length
130	**SECONDARY WINDING**					
131	NSECONDARY	2		2		Secondary winding number of turns
133	**BIAS WINDING**					
134	NBIAS			2		Bias winding number of turns
138	**PRIMARY COMPONENTS SELECTION**					
139	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
140	UVOV Type	UV Only		UV Only		Input Undervoltage/Overvoltage protection type
141	**UNDERVOLTAGE PARAMETERS**					
142	BROWN-IN REQUIRED			95.00	V	Required DC bus brown-in voltage threshold
143	UNDERVOLTAGE ZENER DIODE	BZM55C9V1		BZM55C9V1		Undervoltage protection zener diode
144	VZ			9.10	V	Zener diode reverse voltage
145	VR			6.80	V	Zener diode reverse voltage at the maximum reverse leakage current
146	ILKG			2.00	μA	Zener diode maximum reverse leakage current
147	BROWN-IN ACTUAL			69.22 - 94.65	V	Actual brown-in voltage range using standard resistors
148	BROWN-OUT ACTUAL			62.4 - 84.8	V	Actual brown-out voltage range using standard resistors
149	**OVERVOLTAGE PARAMETERS**					
150	OVERVOLTAGE REQUIRED		Info		V	For UV Only design, overvoltage feature is disabled
151	OVERVOLTAGE DIODE		Info			OV diode is used only for the overvoltage protection circuit
152	VF				V	OV diode forward voltage
153	VRRM				V	OV diode reverse voltage
154	PIV				V	OV diode peak inverse voltage
155	LINE_OVERVOLTAGE				V	For UV Only design, line overvoltage feature is disabled
156	**DC BUS SENSE RESISTORS**					
157	RLS_H			2.62	MΩ	Connect five 523 kOhm DC bus upper sense resistors to the V-pin for the required UV/OV threshold
158	RLS_L			255	kΩ	DC bus lower sense resistor to the V-pin for the required UV/OV threshold

161	**BIAS WINDING**					
162	VBIAS	10.00		10.00	V	Rectified bias voltage
163	VF_BIAS			0.70	V	Bias winding diode forward drop
164	VREVERSE_BIASDIODE			93.33	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
165	CBIAS			22	µF	Bias winding rectification capacitor
166	CBPP			0.47	µF	BPP pin capacitor
170	**SECONDARY COMPONENTS SELECTION**					
171	**FEEDBACK COMPONENTS**					
172	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
173	RFB_LOWER			11.80	kΩ	Lower feedback resistor
174	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
178	**MULTIPLE OUTPUT PARAMETERS**					
179	**OUTPUT 1**					
180	VOUT1			12.00	V	Output 1 voltage
181	IOUT1			1.500	A	Output 1 current
182	POUT1			18.00	W	Output 1 power
183	IRMS_SECONDARY1			4.642	A	Root mean squared value of the secondary current for output 1
184	IRIPPLE_CAP_OUTPUT1			4.393	A	Current ripple on the secondary waveform for output 1
185	NSECONDARY1			2		Number of turns for output 1
186	VREVERSE_RECTIFIER1		Info	95.33	V	Taking into consideration the parasitic voltage ring and assuming this output is connected to the Vo/FWD pin, then the actual stress across the SRFET/FWD pin would be 140.14 V. Given that the absolute maximum FWD pin voltage rating is 150 V, increase the VO
187	SRFET1	AUTO		DMT15H017LPS-13[11]		Secondary rectifier (Logic MOSFET) for output 1
188	NUM_SRFET1	2		2		Number of SRFETs in parallel for output 1
189	VF_SRFET1			0.80	V	SRFET on-time drain voltage for output 1
190	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
191	RDSON_SRFET1			26	mΩ	SRFET on-time drain resistance at 25 degC and VGS = 4.4 V for output 1
192	RTHJA_SRFET1			53.00	°C/W	SRFET max. thermal impedance for output 1
193	PLOSS_SRFET1			137.4	mW	SRFET power loss for output 1 (for each SRFET in parallel)
194	TEMPRISE_SRFET1			7.3	°C	SRFET temperature rise for output 1 (for each SRFET in parallel)
195						
230	PO_TOTAL			18.00	W	Total power of all outputs
231	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
235	**INPUT VOLTAGE SET-POINTS ANALYSIS**					
236	**TOLERANCE CORNER**					
237	USER_VINDC	1000		1000	V	Input DC voltage corner to be evaluated
238	USER_ILIMIT	MIN		1.767	A	Current limit corner to be evaluated
239	USER_LPRIMARY	MIN		427.3	µH	Primary inductance corner to be evaluated
241	**OPERATING CONDITION SELECTION**					
242	POUT	36.00	Info	36.00	W	The value of POUT entered by The user will be used for calculations in this section
243	EFFICIENCY			0.85		Converter efficiency to be evaluated
244	Z FACTOR			0.50		Z-factor to be evaluated
245	FSWITCHING			65183	Hz	Maximum switching frequency at the output power to be evaluated.

[11] The AEC-Q qualified version of the SR FET (MFR Part Number: DMTH15H017LPSWQ) was used for the design.

246	KP			2.939		Measure of continuous/discontinuous mode of operation
247	MODE_OPERATION			DCM		Mode of operation
248	DUTYCYCLE			0.047		Primary switch duty cycle
249	TIME_ON			0.717	µs	Primary switch on-time
250	TIME_OFF			14.625	µs	Primary switch off-time
252	**PRIMARY CURRENT**					
253	IAVG_PRIMARY			0.039	A	Primary switch average current
254	IPEAK_PRIMARY			1.677	A	Primary switch peak current
255	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
256	IRIPPLE_PRIMARY			1.677	A	Primary switch ripple current
257	IRMS_PRIMARY			0.209	A	Primary switch RMS current
259	**MAGNETIC FLUX DENSITY**					
260	BPEAK			2981	Gauss	Peak flux density
261	BMAX			2765	Gauss	Maximum flux density
262	BAC			1382	Gauss	AC flux density (0.5 x Peak to Peak)

Table 7 – DER-1039Q PIXls Spreadsheet.

9 Partial Discharge (PD) and Hi-Pot Testing for Transformer

9.1 Partial Discharge (PD)

Partial discharge (PD) is defined by IEC 60270 as localized electrical discharges that partially bridge the insulation between conductors. It appears as small electrical discharges lasting less than 1 µs. Successful PD testing ensures that high-quality materials are used in the design, thus reducing the risk of failure over time.

Figure 16 shows the test profile used to evaluate the planar transformer of DER-1039Q. The test profile is based on IEC 60664-1:2020.

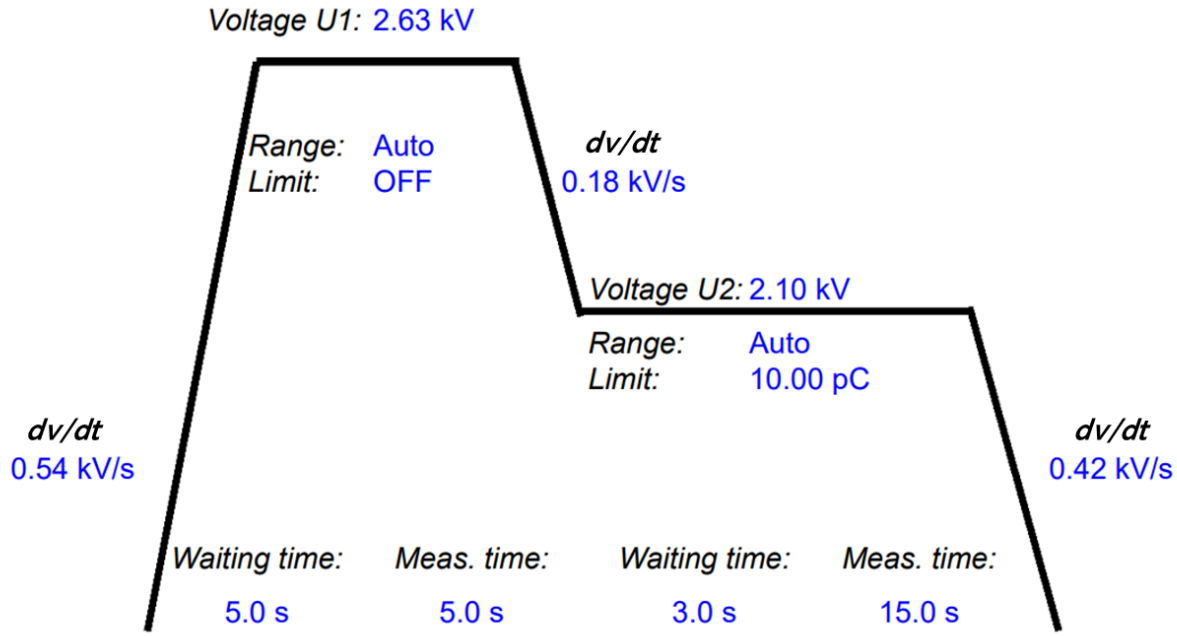


Figure 16 – PD Test Profile of DER-1039Q.

The partial discharge of the planar transformer was measured between nodes 1 to 6 at 25 °C ambient. Nodes 1-4 and nodes 5-6 are shorted. Refer to section 7.1 for the transformer electrical diagram.

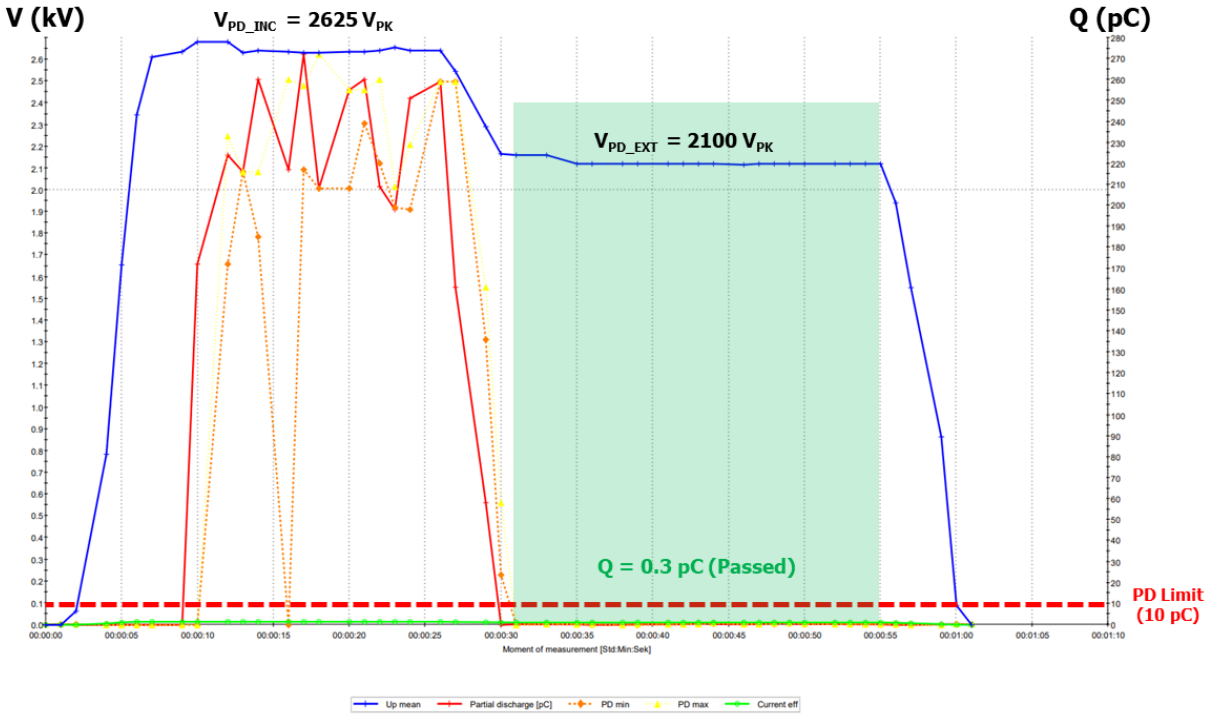


Figure 17 – PD Test Result of DER-1039Q.

9.2 Hi-Pot Testing

Hi-Pot testing measures the dielectric breakdown of the primary-to-secondary isolation used in the transformer. This test is done to assess the ability of the insulation to withstand steady-state working voltage stresses. Hi-Pot testing also checks for the existence of damage in the isolation barrier.

Figure 18 shows the test profile used to evaluate the planar transformer of DER-1039Q.

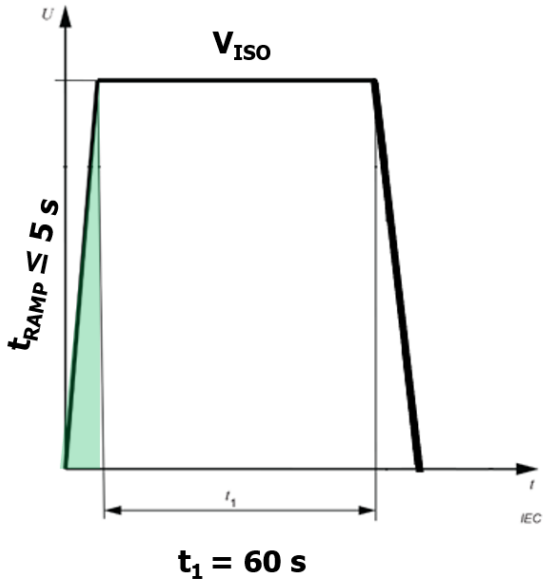


Figure 18 – Hi-Pot Test Profile of DER-1039Q.

The unit under test was tested with an isolation voltage of 4000 V_{RMS} to 6400 V_{RMS} with a 5-second ramp-up and 60-second dwell time. The isolation test was done between nodes 1 to 6 at 25 °C ambient, with nodes 1-4 and 5-6 shorted. Refer to section 7.1 for the transformer electrical diagram.

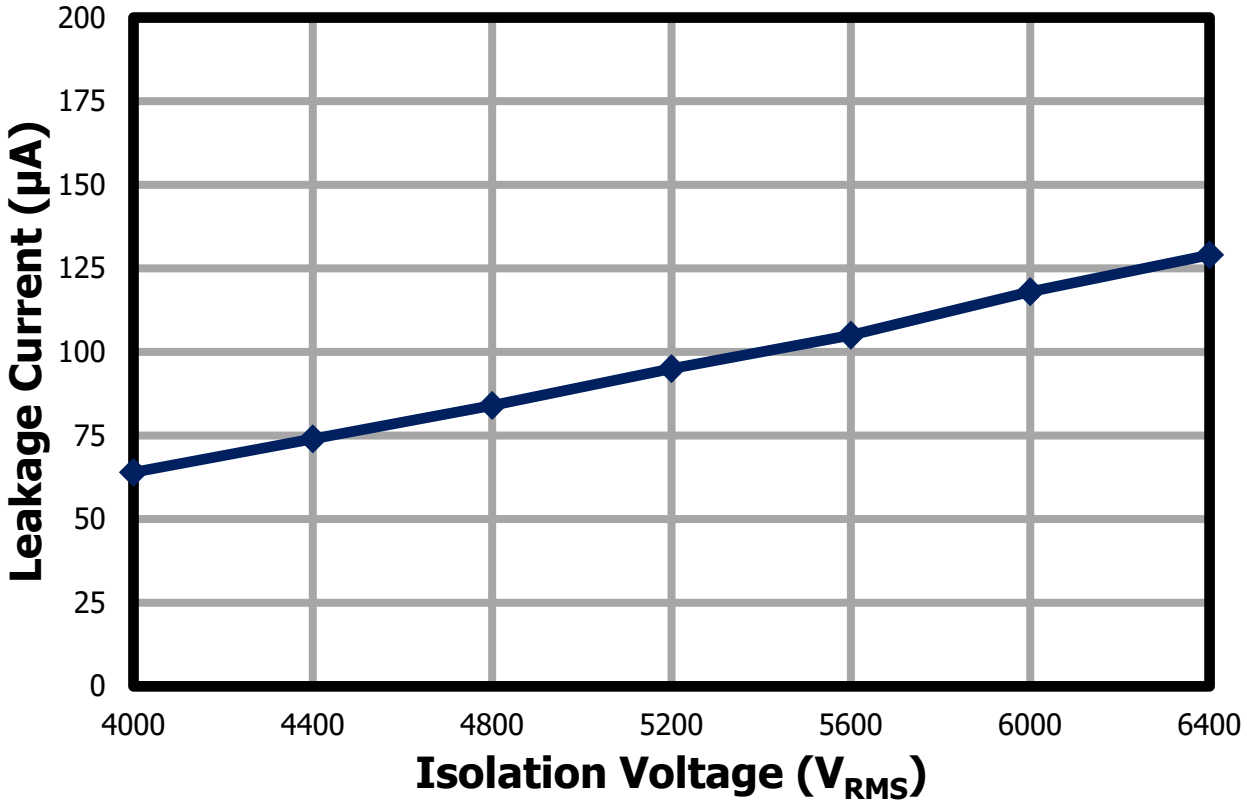


Figure 19 – Isolation Voltage vs. Leakage Current (25 °C Ambient).

Note: The leakage current across the isolation barrier above is due to the primary to secondary coupling capacitance. When the high voltage 60 Hz AC test voltage is applied, current flows through this capacitance (~25 pF). Under DC voltage conditions, this leakage is not present (<3 uA measured).

10 Performance data

Note: 1. Measurements were taken with the unit under test inside a thermal chamber.

2. The DER-1039Q board was placed inside a box within the thermal chamber to eliminate the effects of airflow.

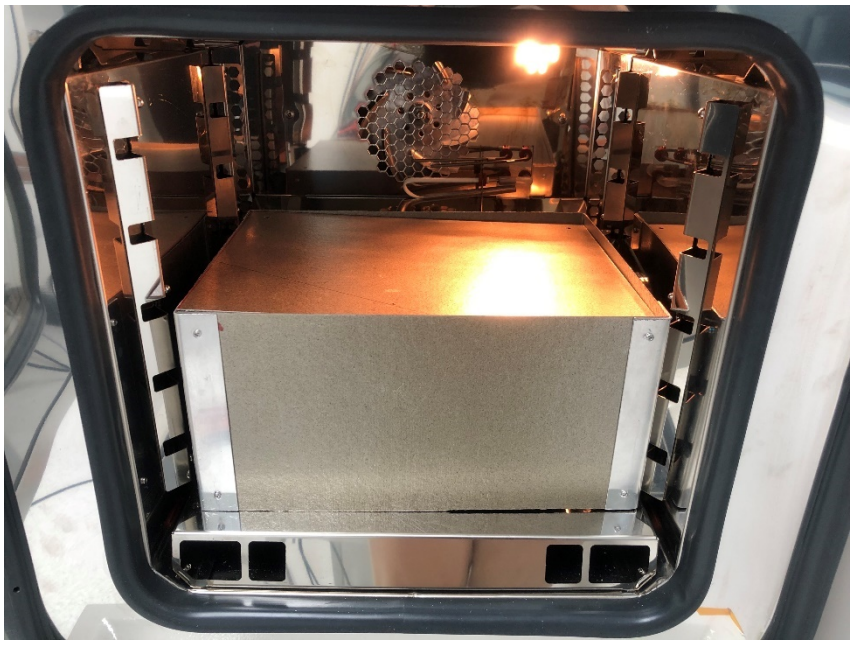


Figure 20 – Unit under test placed inside a box to eliminate the effect of airflow.

3. The DER board was allowed to stabilize for 5 minutes at full load at the start of every test sequence. For each loading condition, the DER-1039Q test board was allowed to stabilize for 1 minute before measurements were taken.

10.1 No-Load Input Power

Figure 21 shows the schematic for the no-load input power measurement setup. The voltmeter was placed before the ammeter to prevent the voltmeter bias current from affecting the input current measurements. A Chroma Digital Power Meter 66205 was used to measure the current and voltage.

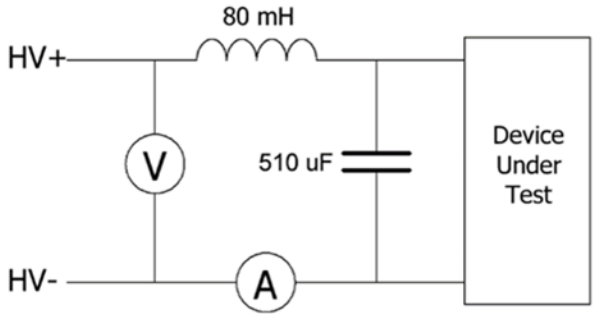


Figure 21 – No-Load Input Power Measurement Diagram.

The unit was allowed to stabilize for ten minutes for each test before measurements were started. The leakage current through the DC-Link capacitor was measured before testing and subtracted from the measured no-load input current. The average voltage across the inductor was assumed to be negligible due to the inductor's very low DCR (40 mΩ) and low input current. AC losses in the inductor were also assumed to be negligible since the input current was DC.

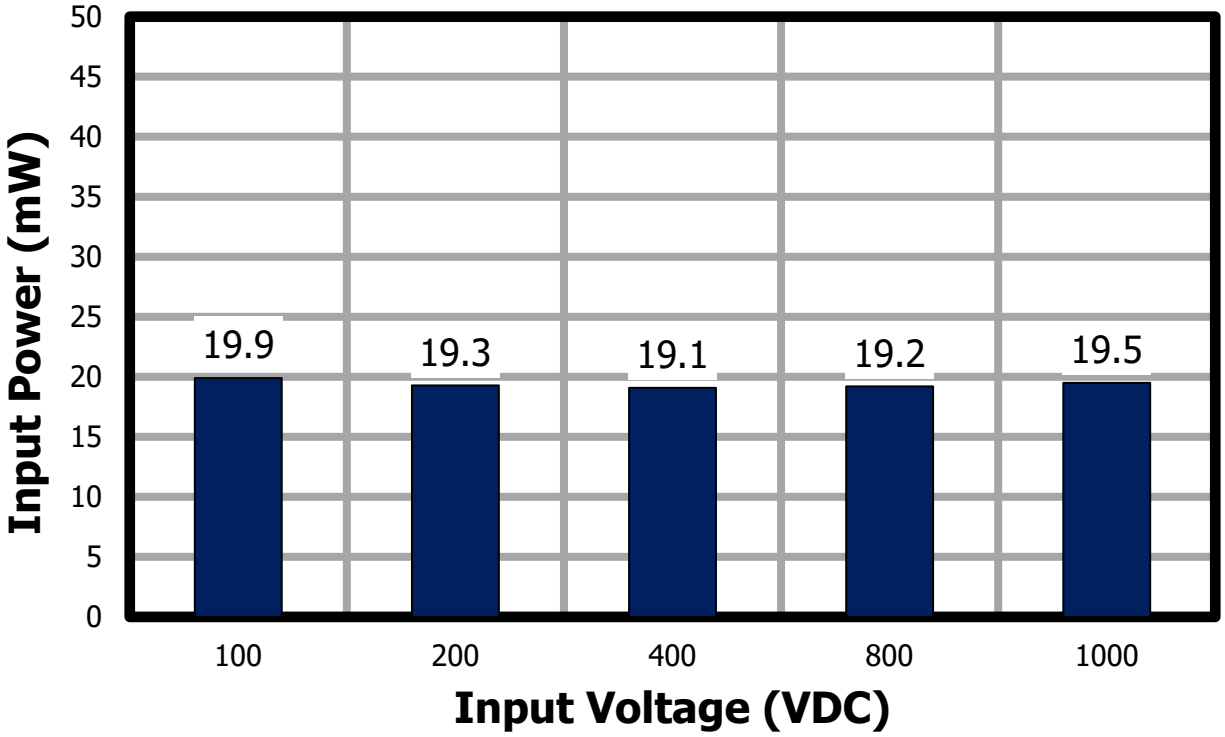


Figure 22 – No-Load Input Power vs. Input Voltage (25 °C Ambient).

10.2 Efficiency

10.2.1 Efficiency Across Line

Efficiency across line describes how input voltage affects the unit's overall efficiency. The points in the graph were taken at 100% load conditions (1.5 A).

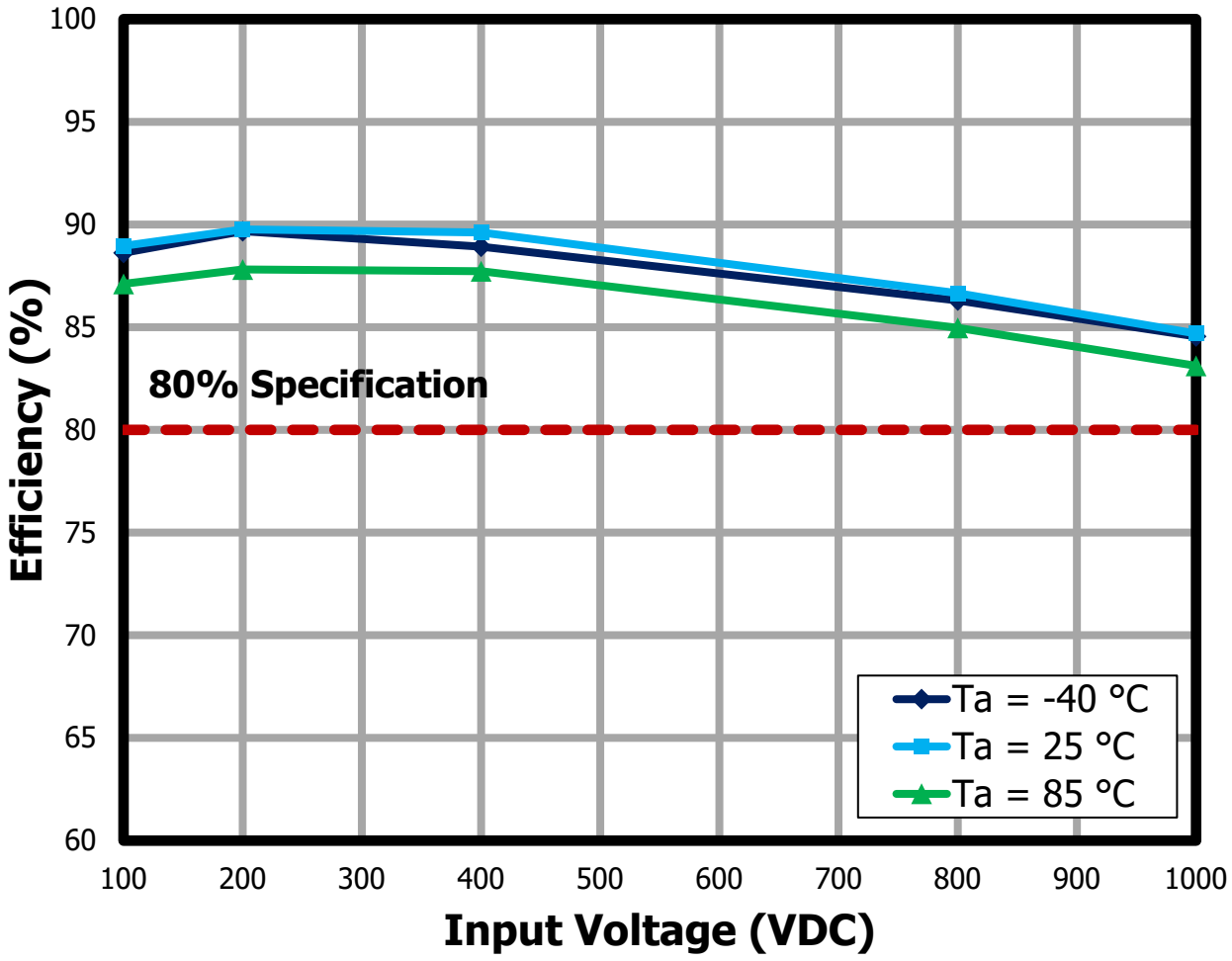


Figure 23 – Full Load Efficiency vs. Input Line Voltage.

10.2.2 Efficiency Across Load

Efficiency across load describes how output loading affects the overall efficiency of the power supply. 100% load was defined at the 1.5 A full load output current.

10.2.2.1 Efficiency Across Load at 85 °C Ambient

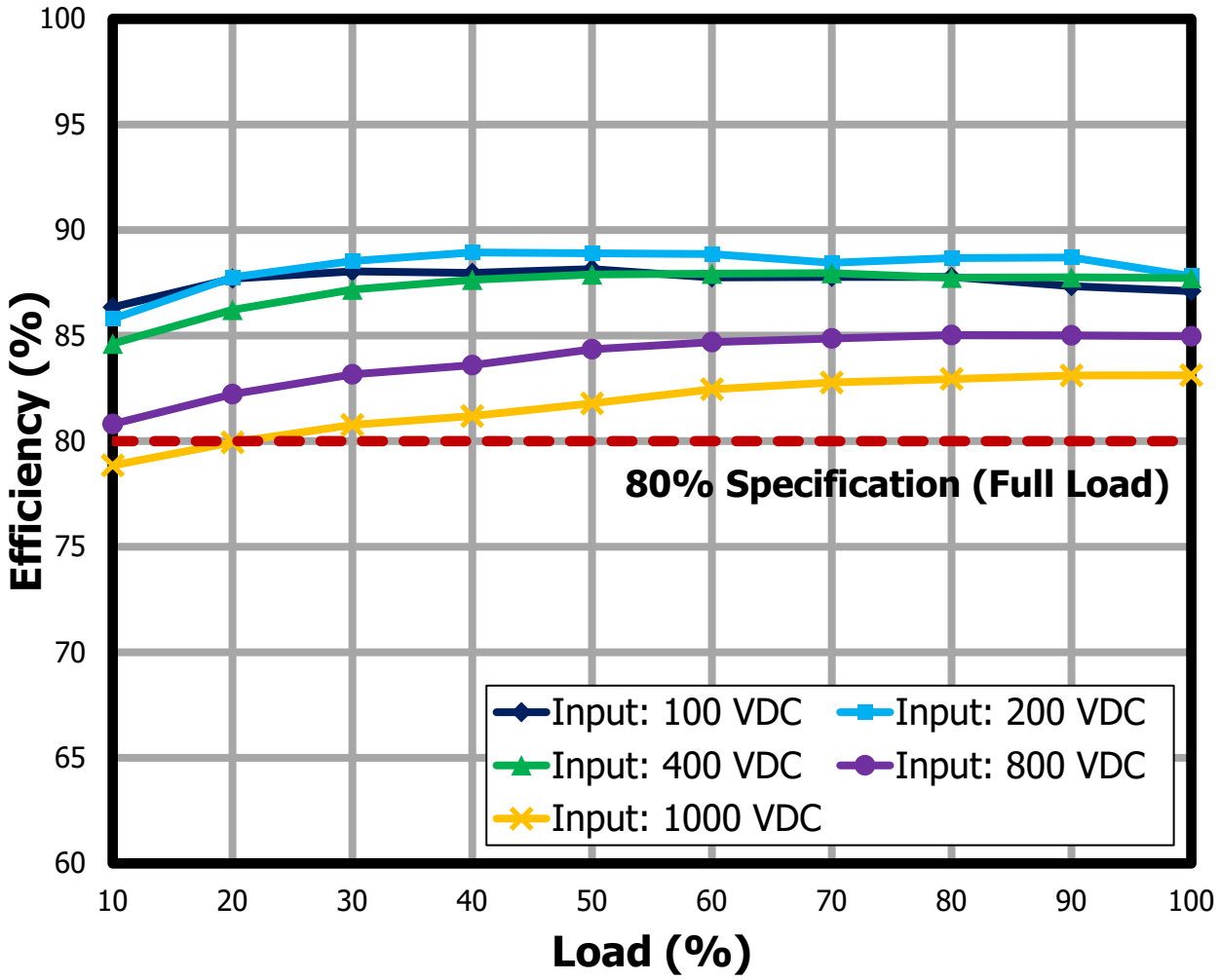


Figure 24 – Efficiency vs. Load at Different Input Voltages (85 °C Ambient).

10.2.2.2 Efficiency Across Load at 25 °C Ambient

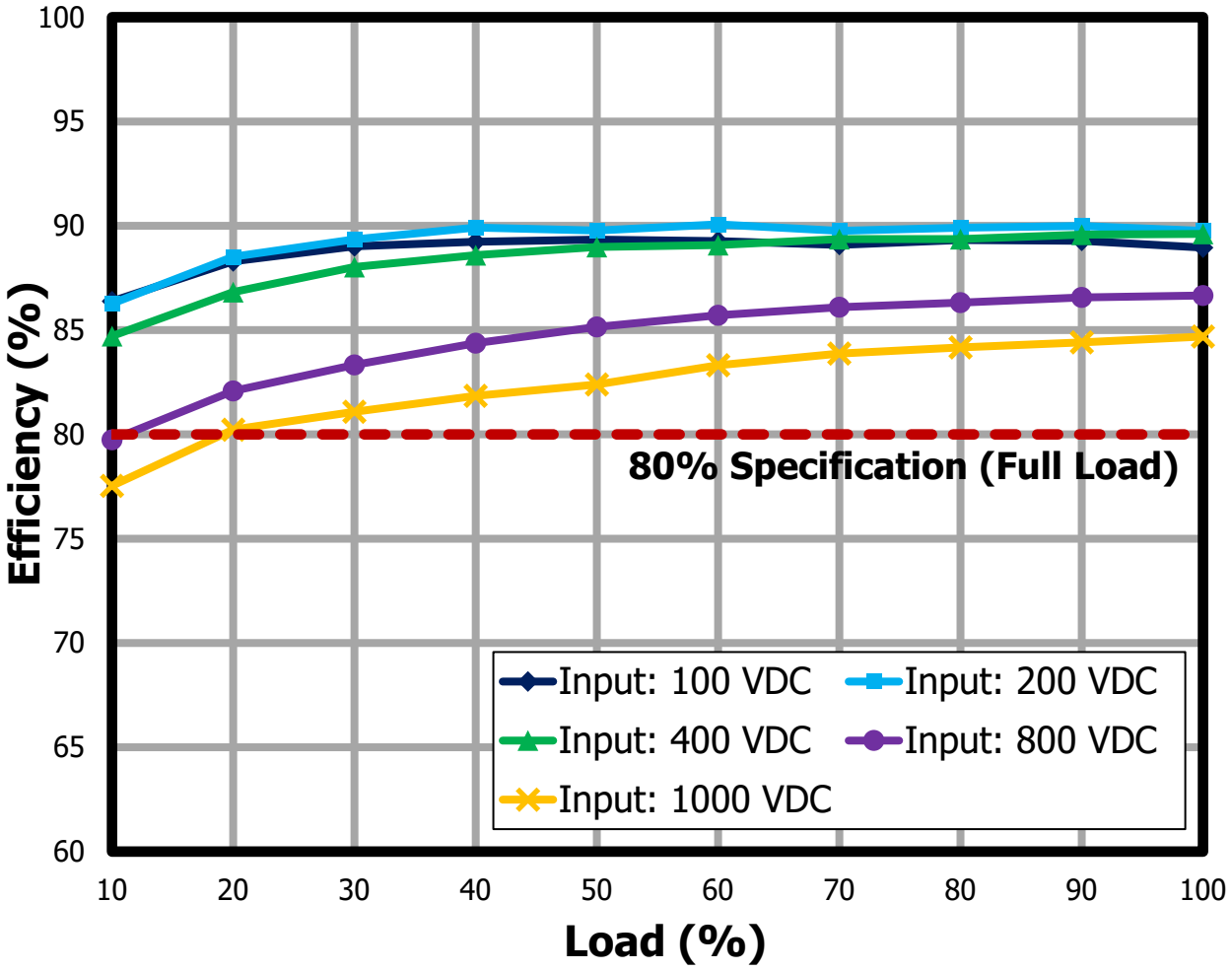


Figure 25 – Efficiency vs. Load at Different Input Voltages (25 °C Ambient).

10.2.2.3 Efficiency Across Load at -40 °C Ambient

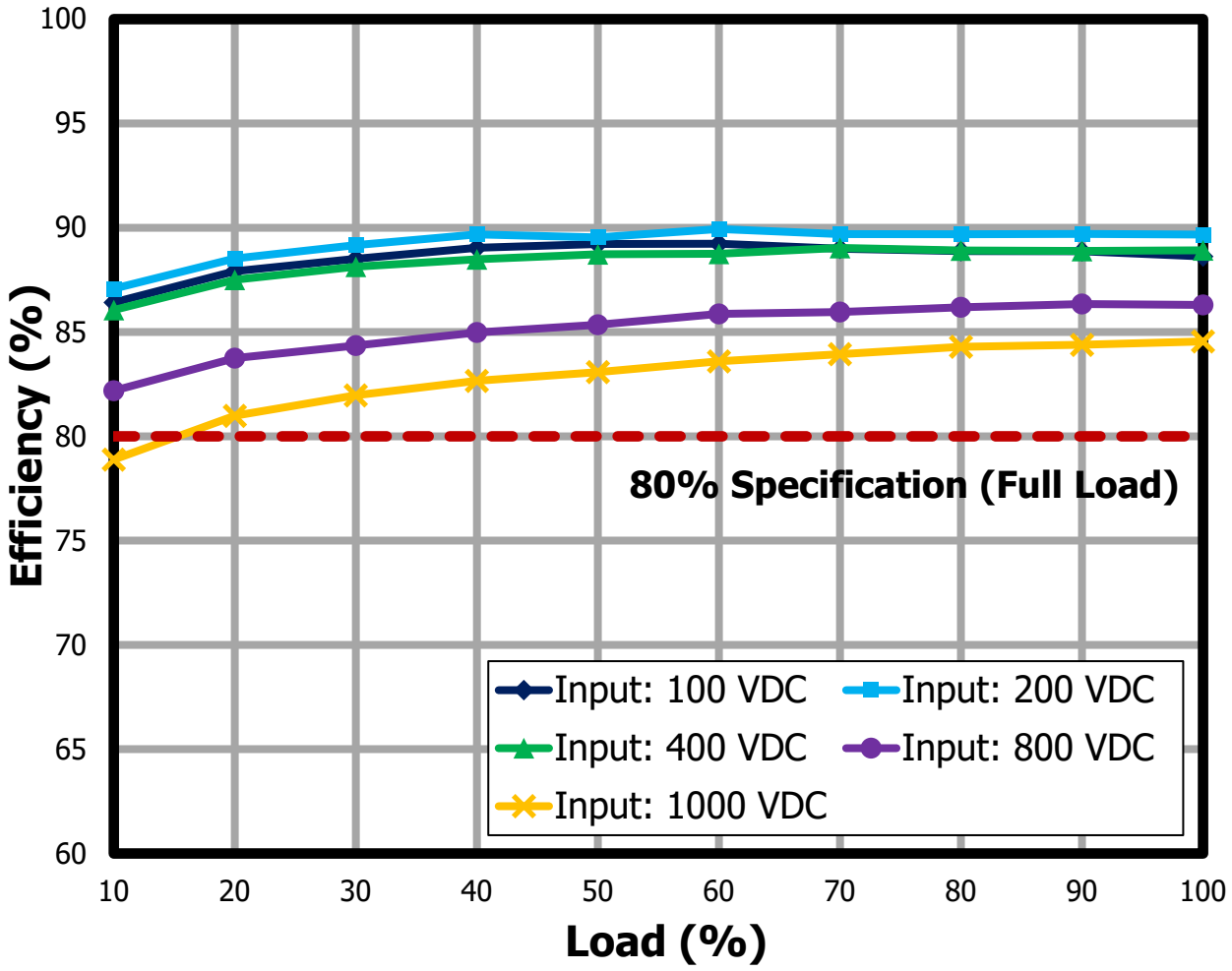


Figure 26 – Efficiency vs. Load at Different Input Voltages (-40 °C Ambient).

10.2.2.4 Efficiency Across Load at 105 °C Ambient

At 105 °C ambient, the output power is derated to 11 W for 800 VDC and further down to 9 W for 1000 VDC[12].

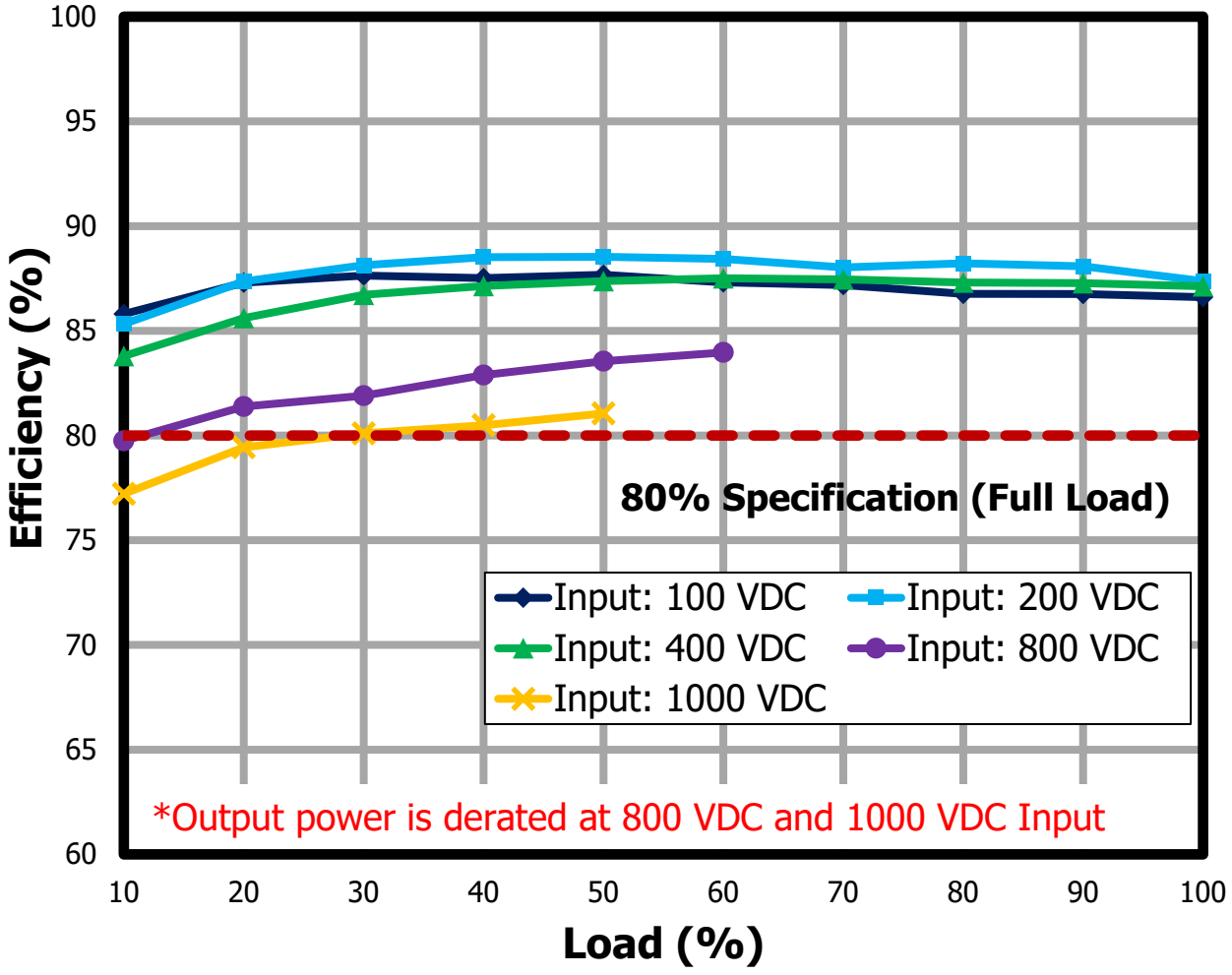


Figure 27 – Efficiency vs. Load at Different Input Voltages (105 °C Ambient).

[12] See Section 13 for power derating curve at 105 °C ambient.

10.3 Line and Load Regulation

10.3.1 Load Regulation

Load regulation describes how a change in load affects output voltage. 100% load was defined at the 1.5 A full load output current.

10.3.1.1 Load Regulation at 85 °C Ambient

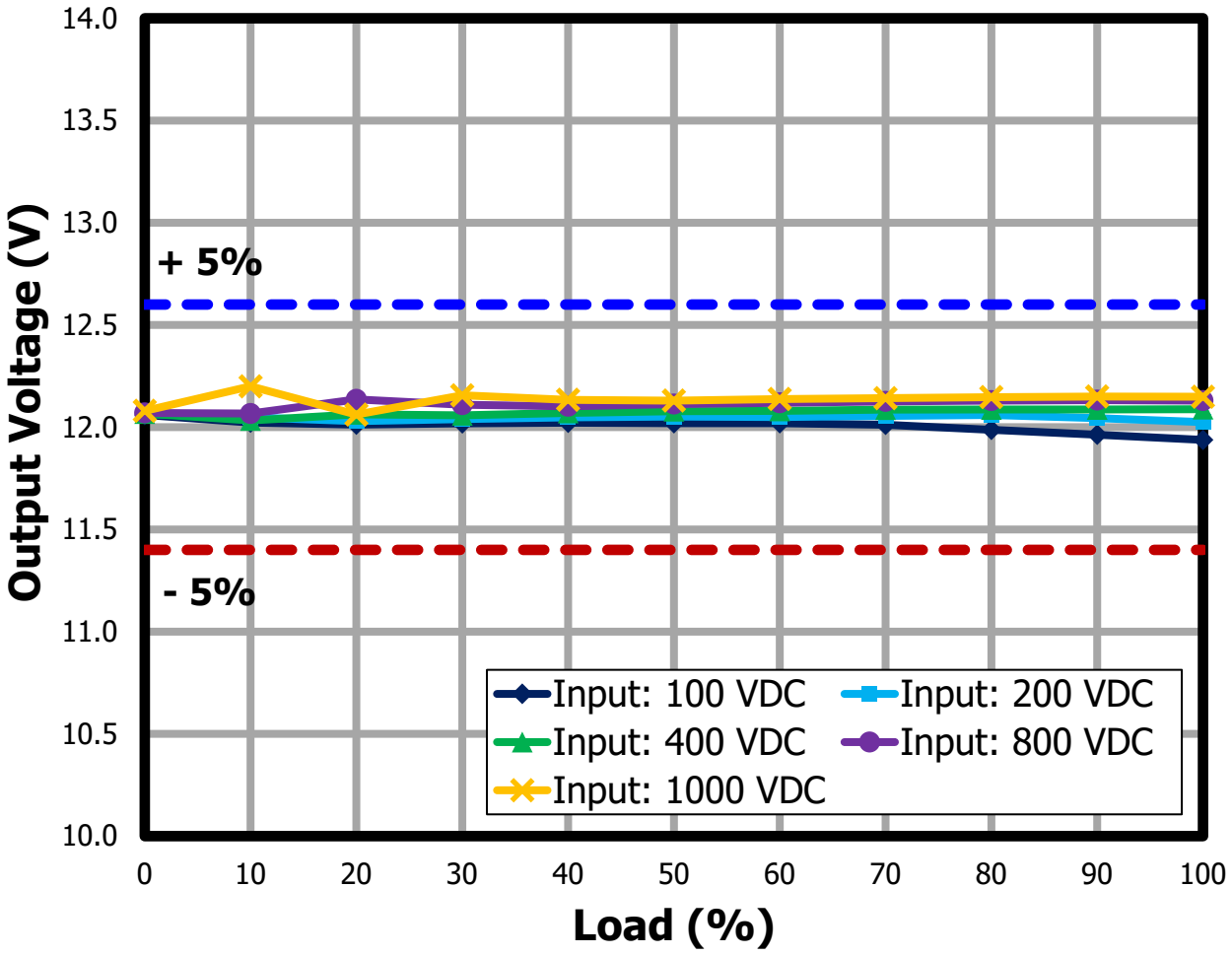


Figure 28 – Output Regulation vs. Load at Different Input Voltages (85 °C Ambient).

10.3.1.2 Load Regulation at 25 °C Ambient

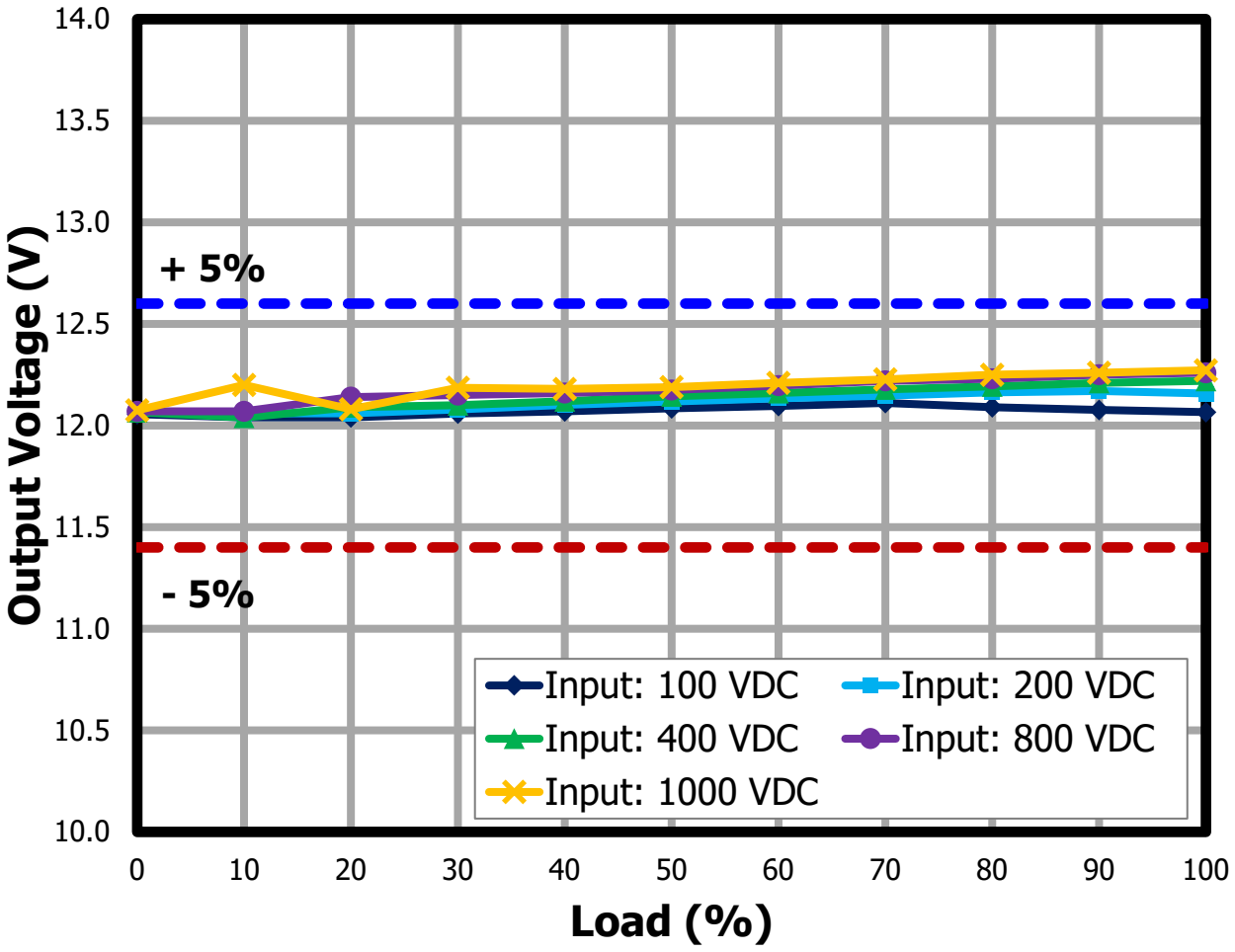


Figure 29 – Output Regulation vs. Load at Different Input Voltages (25 °C Ambient).

10.3.1.3 Load Regulation at -40 °C Ambient

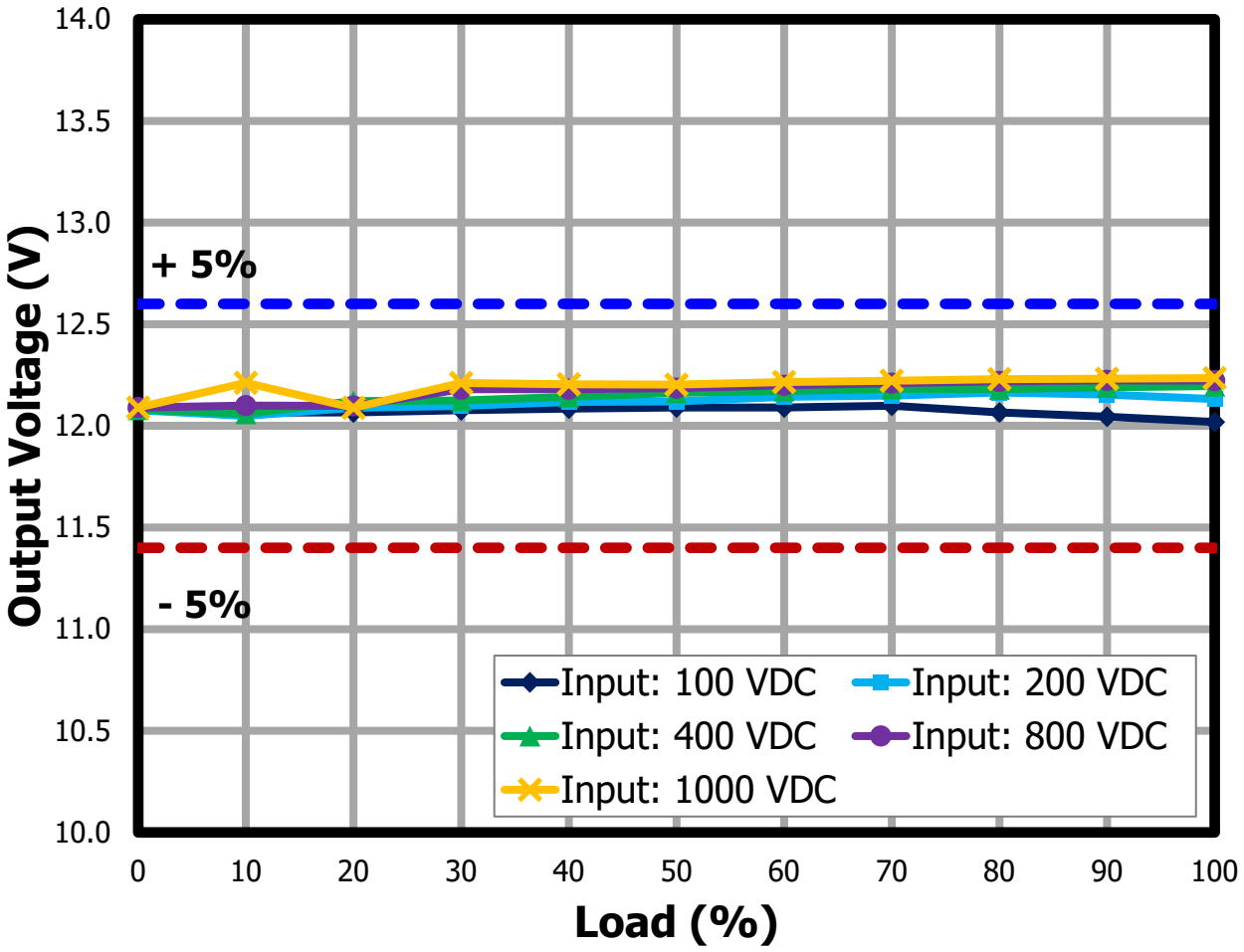


Figure 30 – Output Regulation vs. Load at Different Input Voltages (-40 °C Ambient).

10.3.1.4 Load Regulation at 105 °C Ambient

At 105 °C ambient, the output power is derated to 11 W for 800 VDC and further down to 9 W for 1000 VDC[13].

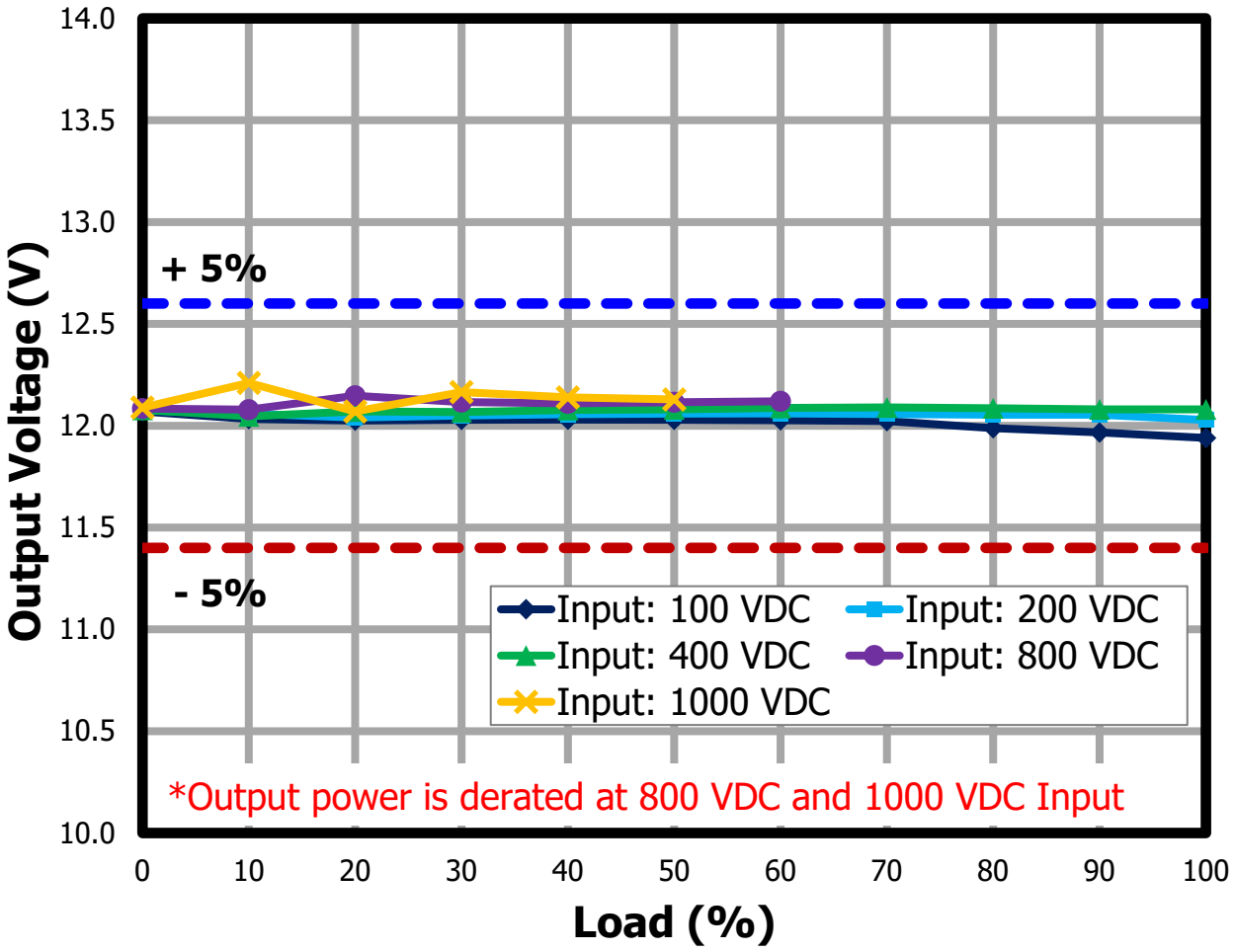


Figure 31 – Output Regulation vs. Load at Different Input Voltages (105 °C Ambient).

[13] See Section 13 for power derating curve at 105 °C ambient.

10.3.2 Line Regulation

Line regulation describes how a change in input voltage affects the output voltage. The points in the graph were taken at 100% (1.5 A) load.

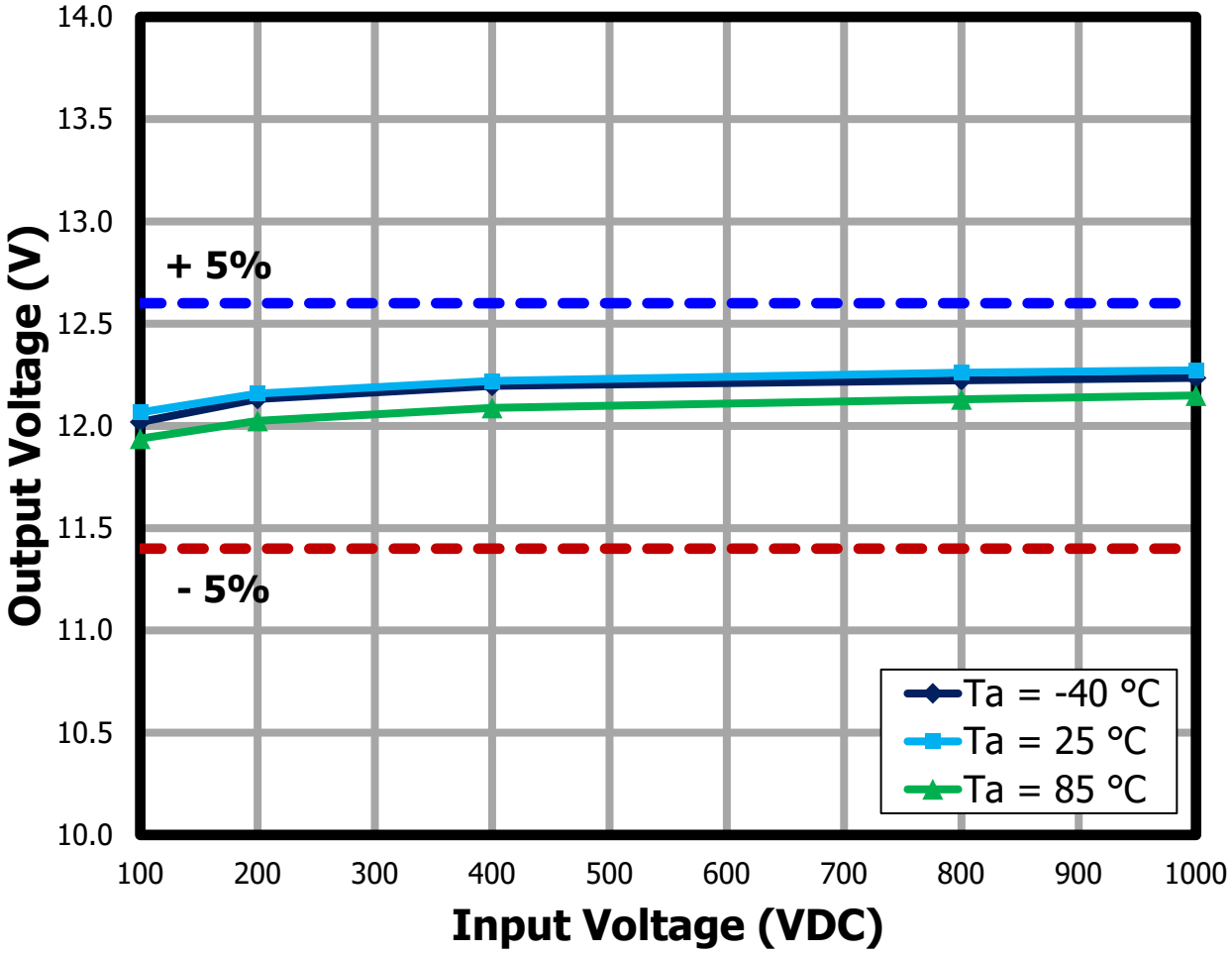


Figure 32 – Output Voltage vs Input Voltage at Full Load (1.5 A).

11 Thermal Performance

11.1 Thermal Data at 85 °C Ambient

The unit was placed inside a thermal chamber and was allowed to stabilize at 100% load for at least 1 hour. Figure 20 shows the test setup for thermal measurement.

11.1.1 18 W Continuous Output Power

Critical Components	Temperature (°C)		
	100 VDC	800 VDC	1000 VDC
INN3949FQ (IC1)	100	121	134[14]
Primary Snubber Resistor (R2)	96.1	96.9	100
Damping Resistor (R5 and R6)	100	102	107
Transformer Winding (T1)	110	113	118
Transformer Core (T1)	105	110	115
SR MOSFET (Q1)	100	108	112
SR MOSFET (Q2)	100	108	111
Secondary Snubber Resistor (R10 and R11)	100	113	119
Output Capacitor (C18)	96.3	108	104
Output Current Sense Resistor (R19 and R20)	94.8	101	102

Table 8 – Thermal Data of 18 W Continuous Output Power at 85 °C at Different Input Voltages.

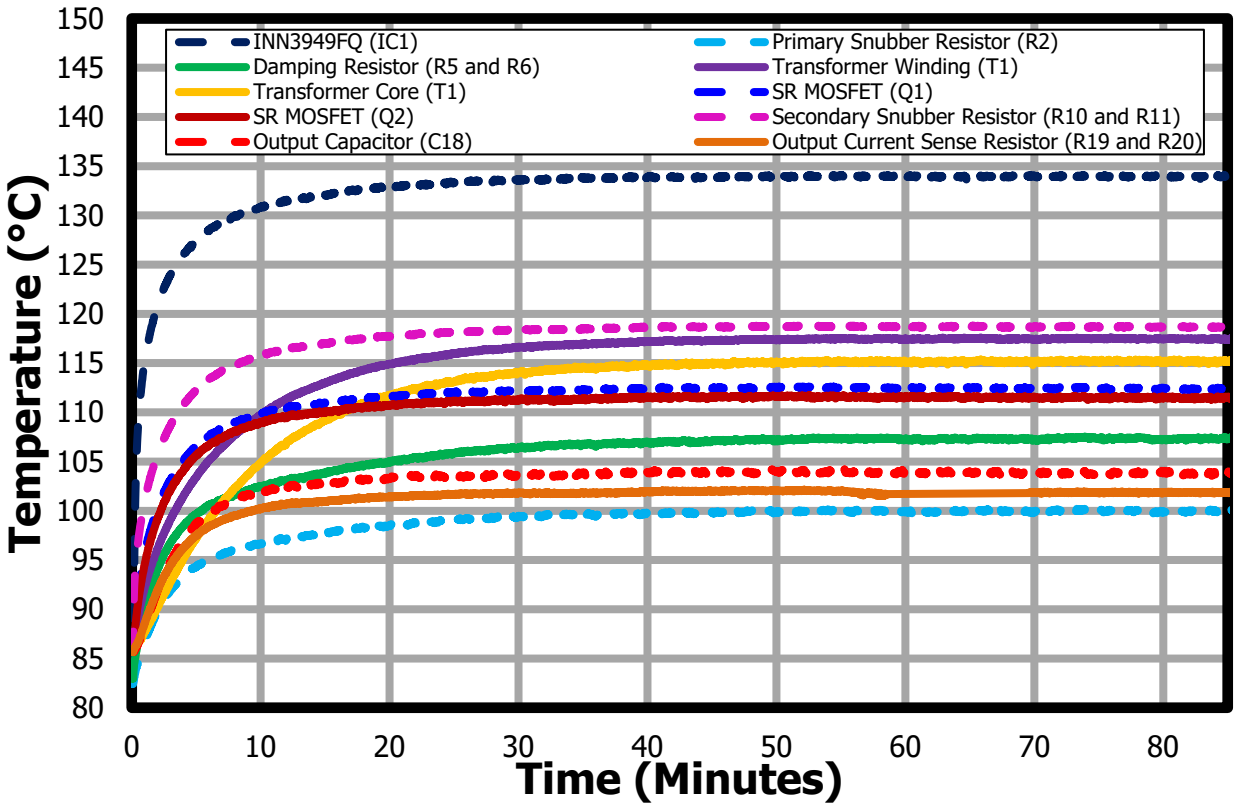


Figure 33 – Component Temperatures at 85 °C Ambient, 1000 VDC Input, 1.5 A Load.

[14] Increasing the cooling area, or adding a heatsink or thermal pad to enclosure is recommended to maintain device temperature below 125 °C.

11.1.2 Operating Time of Peak Output Power at 85 °C Ambient

This test determines the maximum operating time of the peak output power at 85 °C ambient before overtemperature protection (OTP) is triggered. The unit was placed inside a thermal chamber and stabilized for 30 minutes at 1000 VDC with no load before applying peak output current. Data was collected until overtemperature protection (OTP) was triggered.

11.1.2.1 36 W Peak Output Power

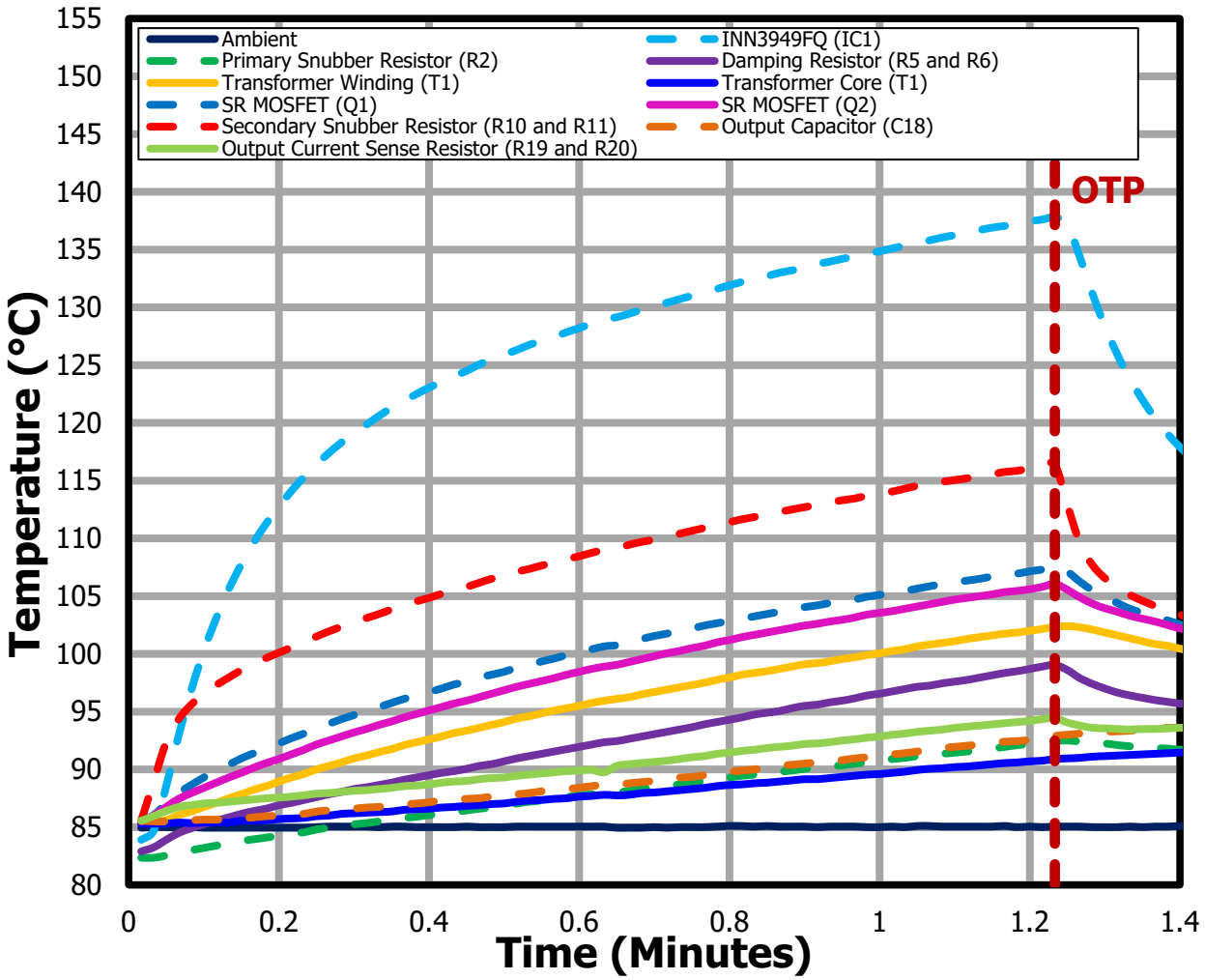


Figure 34 – Component Temperatures at 85 °C Ambient, 1000 VDC Input, 3 A Load.

11.1.2.2 24 W Peak Output Power

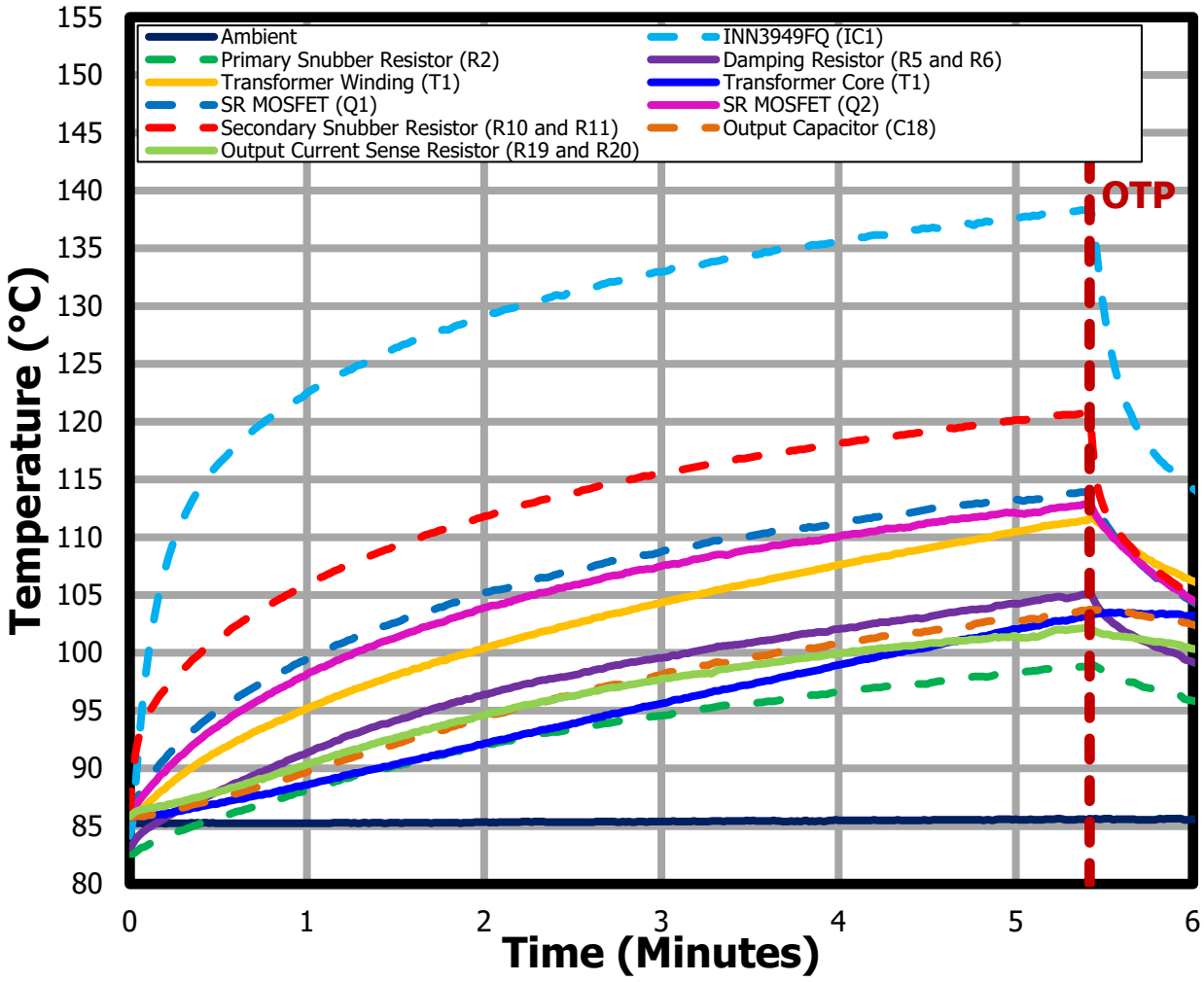


Figure 35 – Component Temperatures at 85 °C Ambient, 1000 VDC Input, 2 A Load.

11.2 Thermal Data at 25 °C Ambient

11.2.1 18 W Continuous Output Power

The following thermal scans were captured using a Fluke thermal imager after soaking the power supply in an enclosure (to minimize the effect of airflow) for 1 hour.

Critical Components	Temperature (°C)		
	100 VDC	800 VDC	1000 VDC
INN3949FQ (IC1)	42.1	65.0	80.2
Primary Snubber Resistor	44.6	44.4	47.6
Damping Resistor (R5 and R6)	45.6	46.5	49.5
Transformer Winding (T1)	52.3	55.1	58.5
Transformer Core (T1)	48.5	53.6	56.6
SR MOSFET (Q1)	39.3	50.4	55.4
SR MOSFET (Q2)	39.8	48.1	52.4
Secondary Snubber Resistor (R10 and R11)	38.8	55.1	63.5
Output Capacitor (C19)	39.3	42.6	45.9
Output Current Sense Resistor (R19 and R20)	36.5	42.8	46.4

Table 9 – Thermal Data at 25 °C at Different Input Voltages.

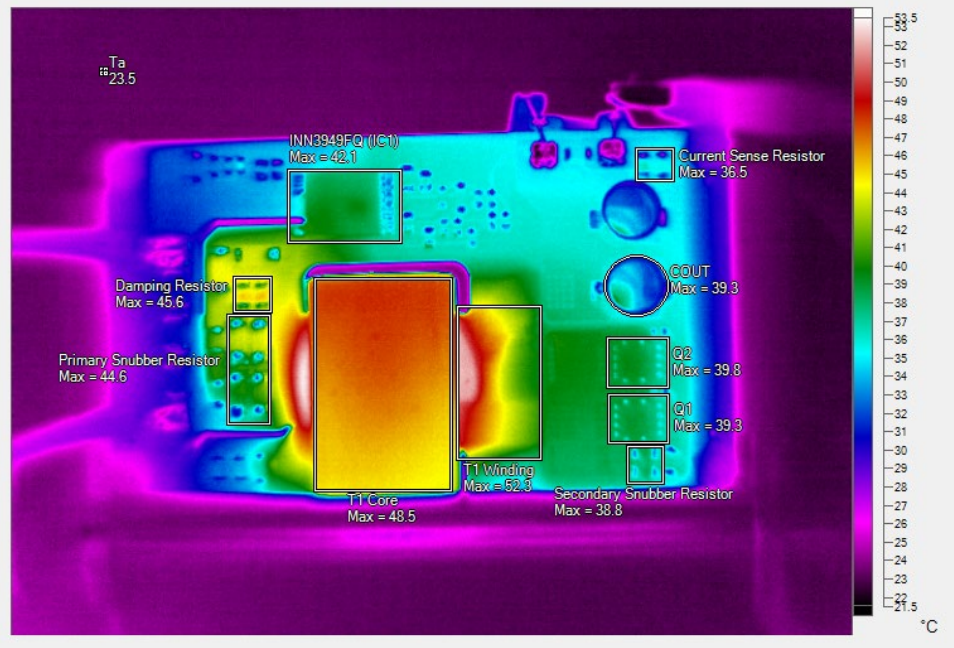


Figure 36 – Thermal Scan at 100 VDC Input, 1.5 A Load.

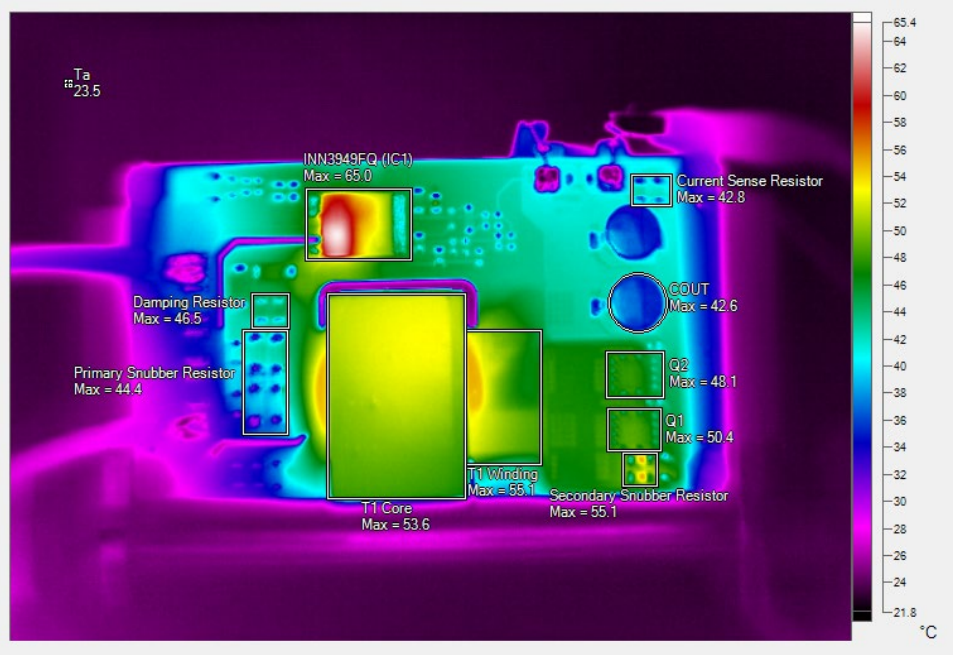


Figure 37 – Thermal Scan at 800 VDC Input, 1.5 A Load.

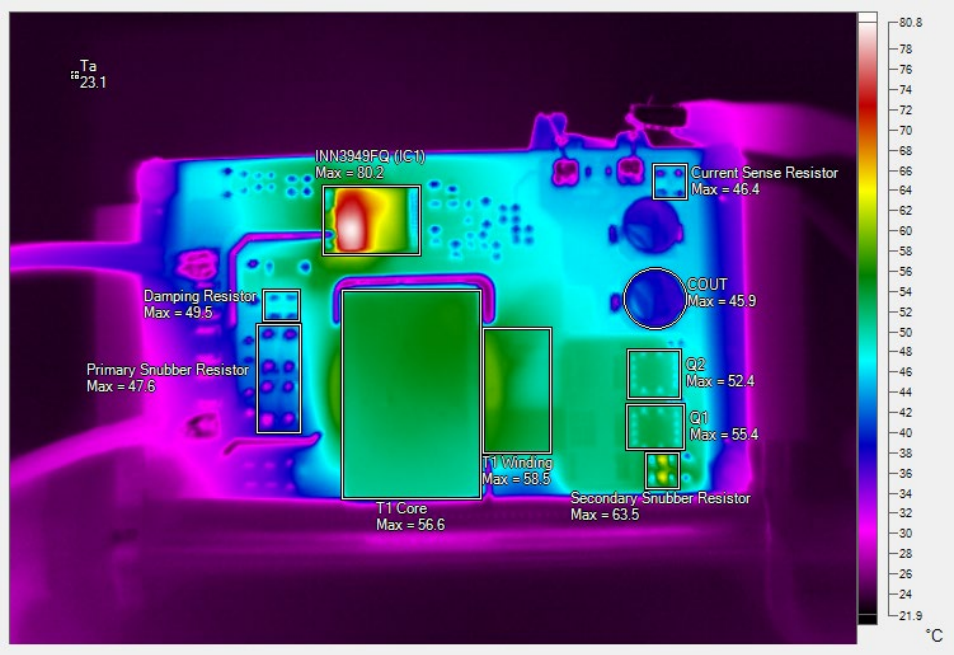


Figure 38 – Thermal Scan at 1000 VDC Input, 1.5 A Load.

12 Waveforms

12.1 Start-Up Waveforms

The following measurements were taken by connecting the unit to a fully charged DC-link capacitor[15] at different input voltages. A constant resistance load configuration was used for all start-up tests.

12.1.1 Output Voltage and Current at 25 °C Ambient[16]

12.1.1.1 18 W Continuous Output Power

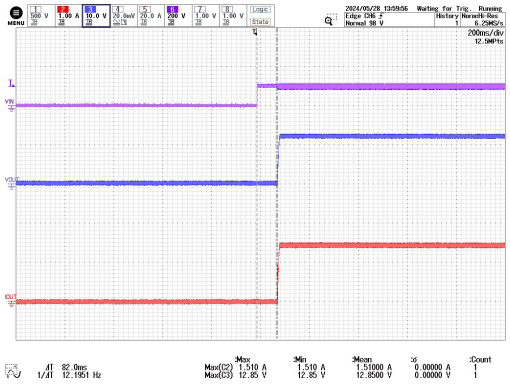


Figure 39 – Output Voltage and Current.
100 VDC, 8 Ω Load.
CH6: V_{IN}, 200 V / div.
CH3: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 200 ms / div.

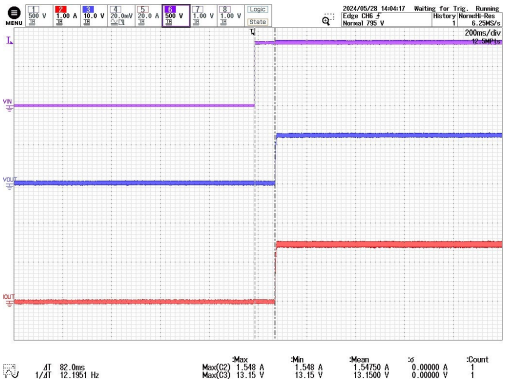


Figure 40 – Output Voltage and Current.
800 VDC, 8 Ω Load.
CH6: V_{IN}, 500 V / div.
CH3: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 200 ms / div.

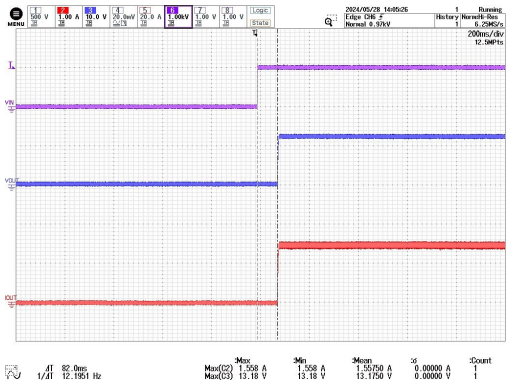


Figure 41 – Output Voltage and Current.
1000 VDC, 8 Ω Load.
CH6: V_{IN}, 1000 V / div.
CH3: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 200 ms / div.

[15] Inrush current was limited by adding a 10 Ω series resistor between the DC-link capacitor and the unit under test.
[16] Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.

12.1.1.2 36 W Peak Output Power

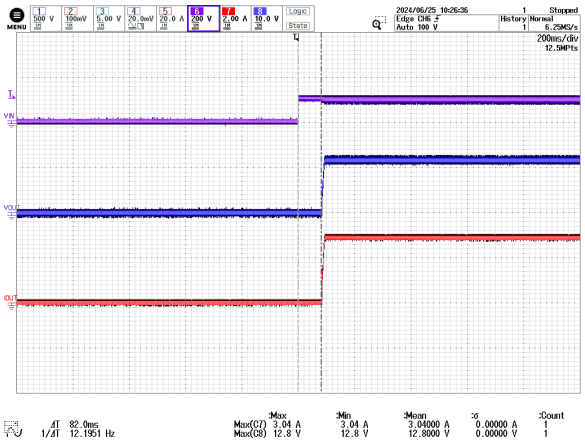


Figure 42 – Output Voltage and Current.
100 VDC, 4 Ω Load.
CH6: V_{IN}, 200 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 2 A / div.
Time: 200 ms / div.

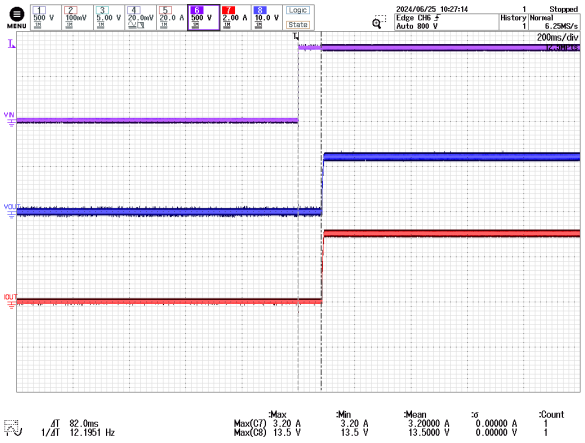


Figure 43 – Output Voltage and Current.
800 VDC, 4 Ω Load.
CH6: V_{IN}, 500 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 2 A / div.
Time: 200 ms / div.

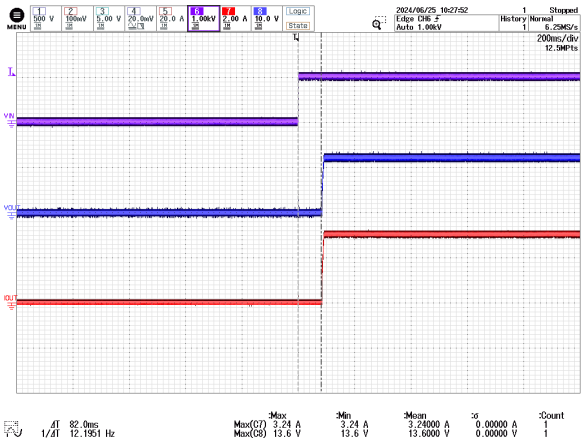


Figure 44 – Output Voltage and Current.
1000 VDC, 4 Ω Load.
CH6: V_{IN}, 1000 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 2 A / div.
Time: 200 ms / div.

12.1.1.3 24 W Peak Output Power

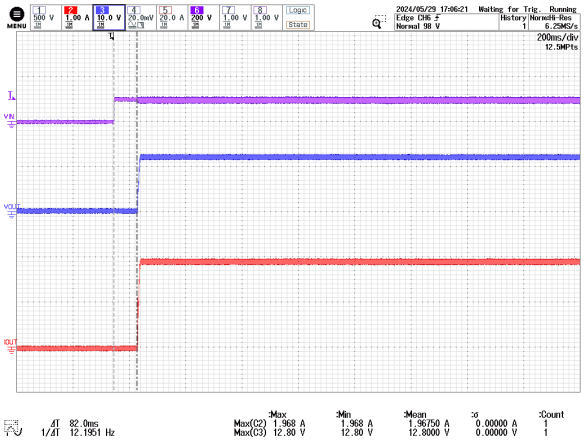


Figure 45 – Output Voltage and Current.
100 VDC, 6 Ω Load.
CH6: V_{IN}, 200 V / div.
CH3: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 200 ms / div.

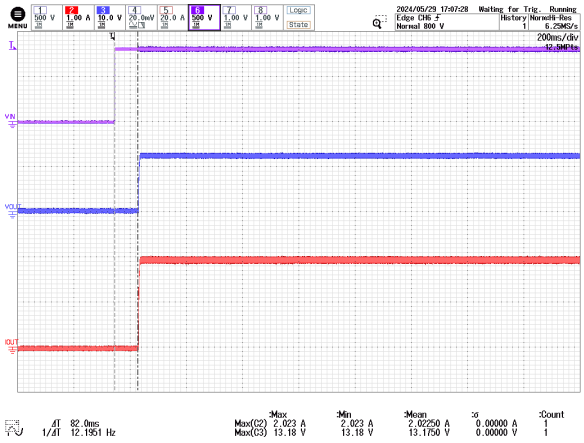


Figure 46 – Output Voltage and Current.
800 VDC, 6 Ω Load.
CH6: V_{IN}, 500 V / div.
CH3: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 200 ms / div.

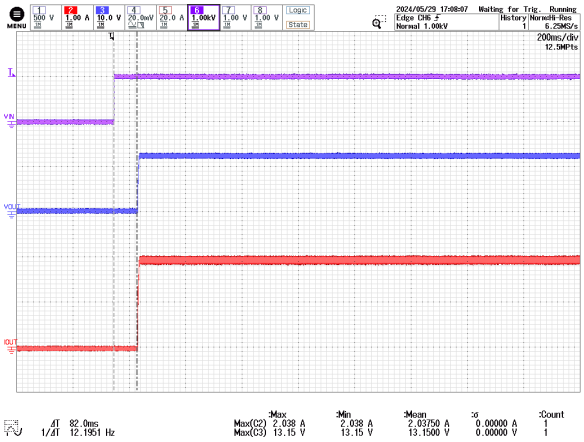


Figure 47 – Output Voltage and Current.
1000 VDC, 6 Ω Load.
CH6: V_{IN}, 1000 V / div.
CH3: V_{OUT}, 10 V / div.
CH2: I_{OUT}, 1 A / div.
Time: 200 ms / div.

12.1.2 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient[17,18]

12.1.2.1 18 W Continuous Output Power

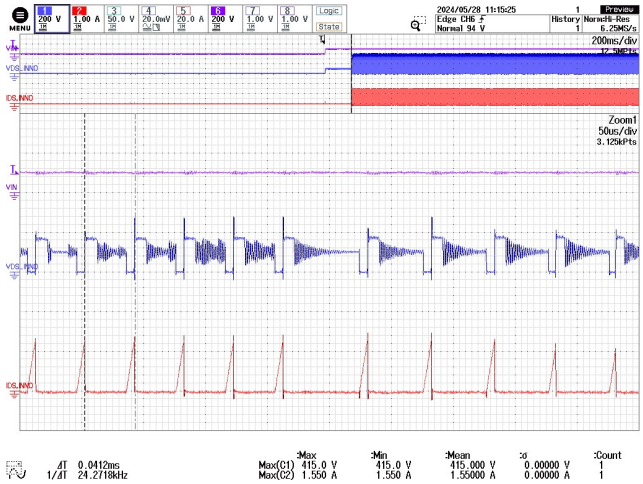


Figure 48 – INN3949FQ Drain Voltage and Current.
100 VDC, 8 Ω Load.
CH1: $V_{DS,INNO}$, 200 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

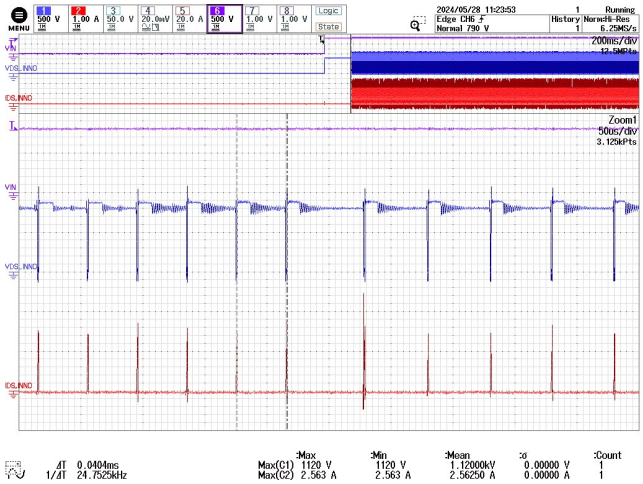


Figure 49 – INN3949FQ Drain Voltage and Current.
800 VDC, 8 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

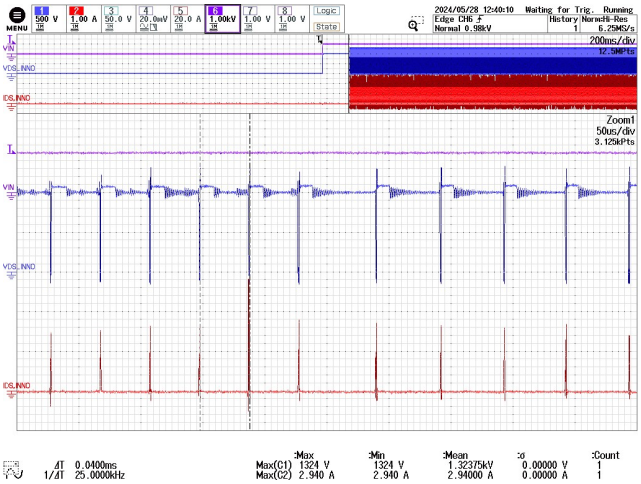


Figure 50 – INN3949FQ Drain Voltage and Current.
1000 VDC, 8 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

[17] The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[18] Current waveforms were measured using a Yokogawa current probe.

12.1.2.2 36 W Peak Output Power

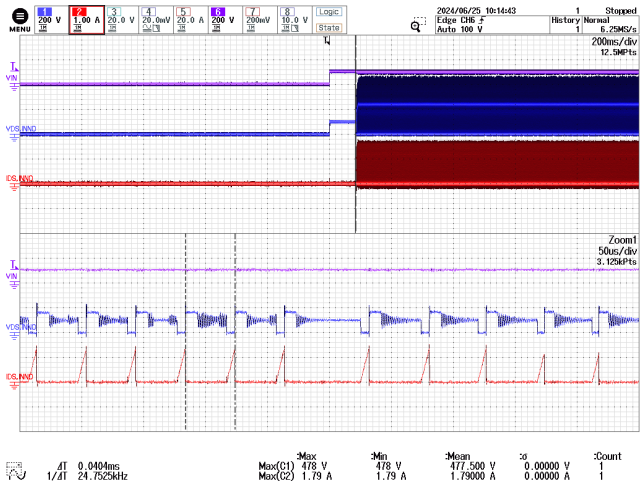


Figure 51 – INN3949FQ Drain Voltage and Current.
100 VDC, 4 Ω Load.
CH1: $V_{DS,INNO}$, 200 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

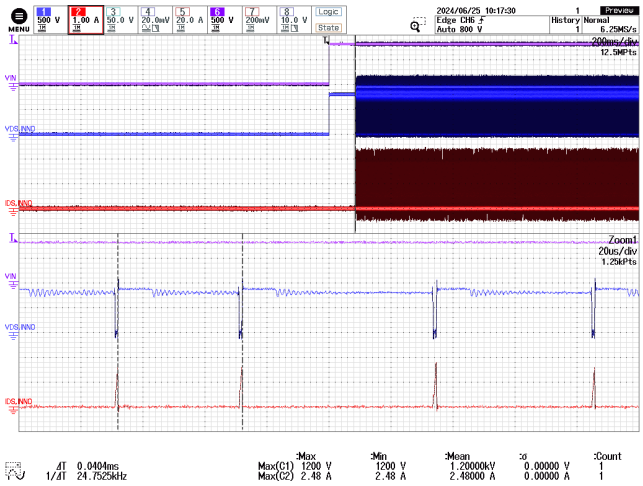


Figure 52 – INN3949FQ Drain Voltage and Current.
800 VDC, 4 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

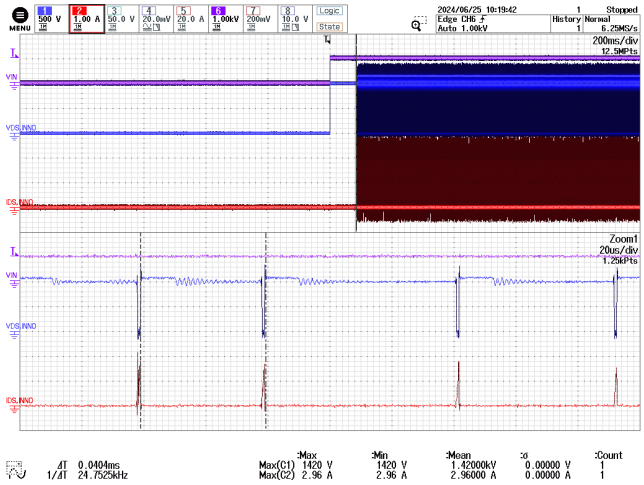


Figure 53 – INN3949FQ Drain Voltage and Current.
1000 VDC, 4 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.1.2.3 24 W Peak Output Power

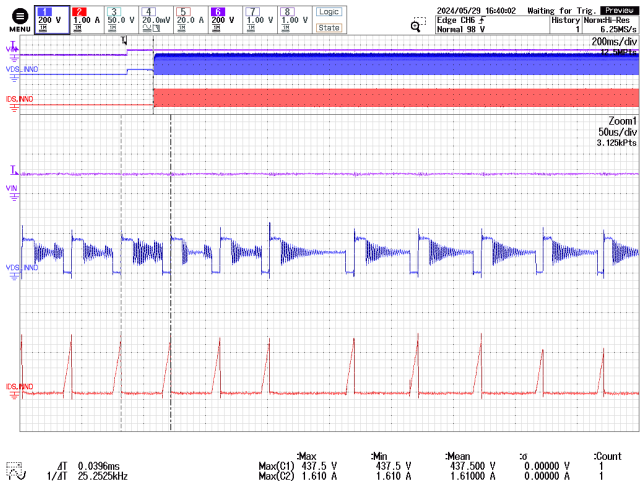


Figure 54 – INN3949FQ Drain Voltage and Current.
100 VDC, 6 Ω Load.
CH1: $V_{DS,INNO}$, 200 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

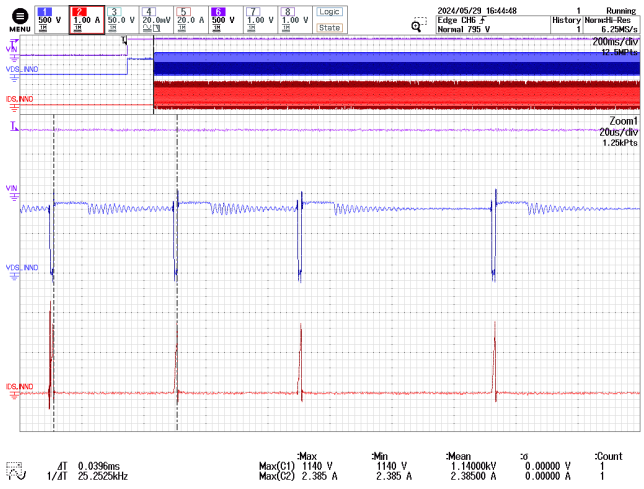


Figure 55 – INN3949FQ Drain Voltage and Current.
800 VDC, 6 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

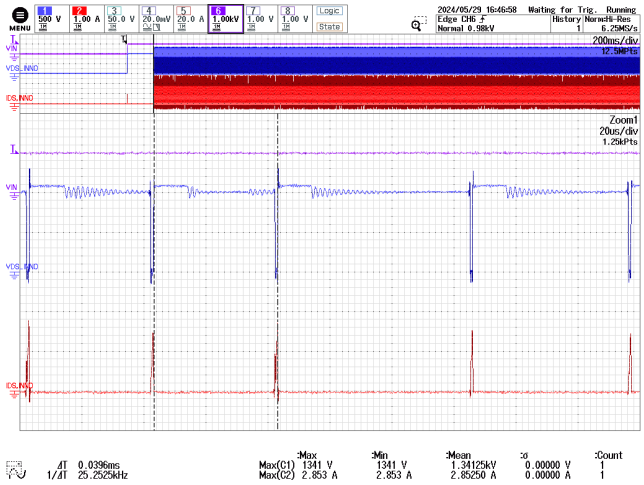


Figure 56 – INN3949FQ Drain Voltage and Current.
1000 VDC, 6 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.1.3 SR FET Drain Voltage and Current at 25 °C Ambient[19,20]

12.1.3.1 18 W Continuous Output Power

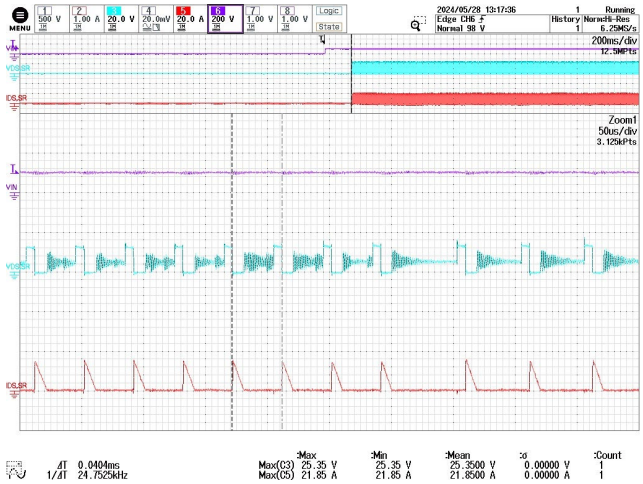


Figure 57 – SR FET Drain Voltage and Current.
100 VDC, 8 Ω Load.
CH3: $V_{DS,SR}$, 20 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

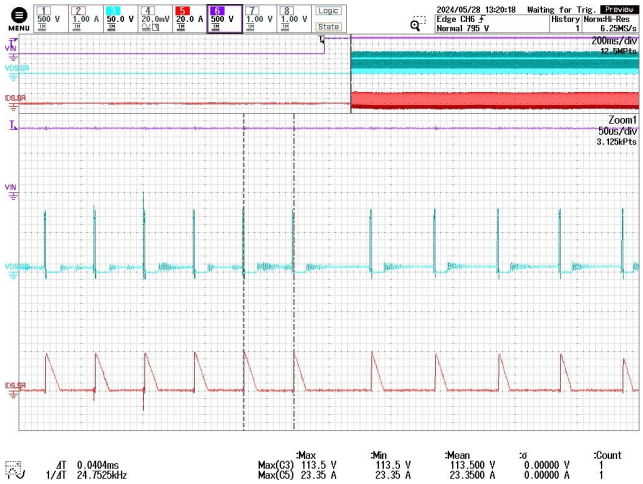


Figure 58 – SR FET Drain Voltage and Current.
800 VDC, 8 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

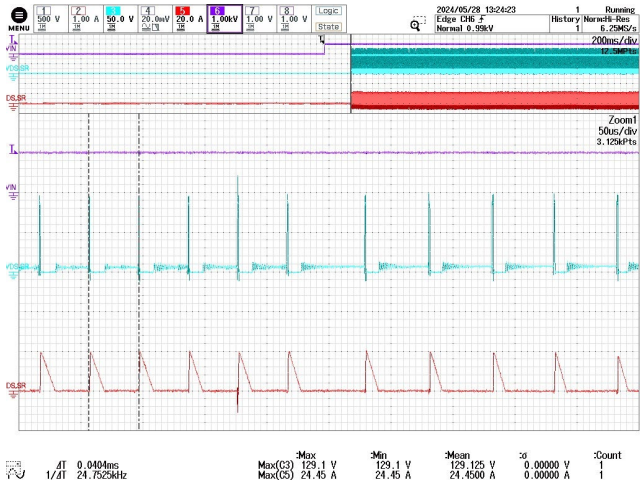


Figure 59 – SR FET Drain Voltage and Current.
1000 VDC, 8 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

[19] The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[20] Current waveforms were measured using a Rogowski coil.

12.1.3.2 36 W Peak Output Power

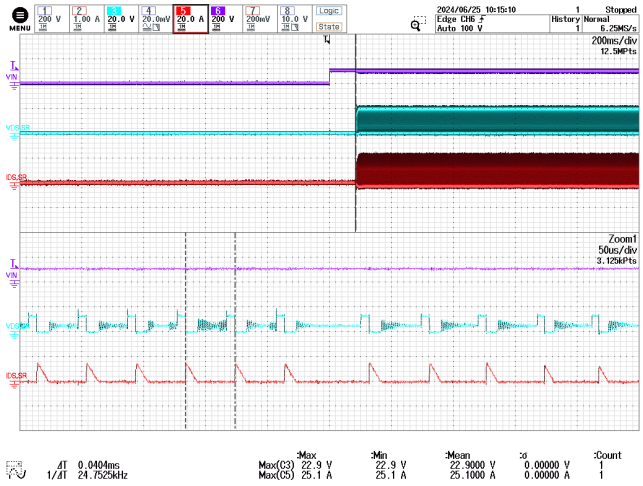


Figure 60 – SR FET Drain Voltage and Current.
100 VDC, 4 Ω Load.
CH3: $V_{DS,SR}$, 20 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

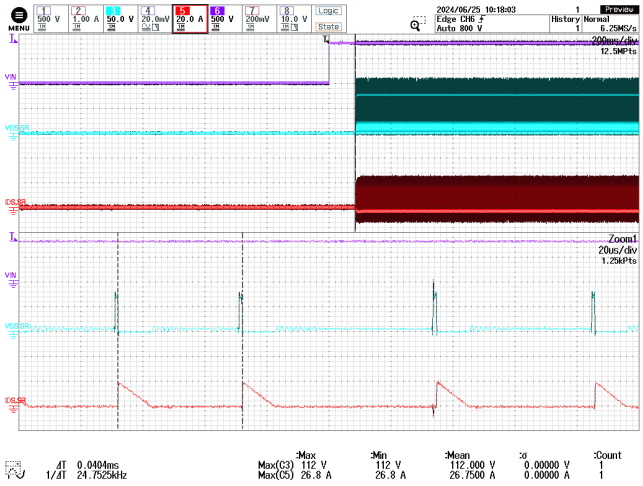


Figure 61 – SR FET Drain Voltage and Current.
800 VDC, 4 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

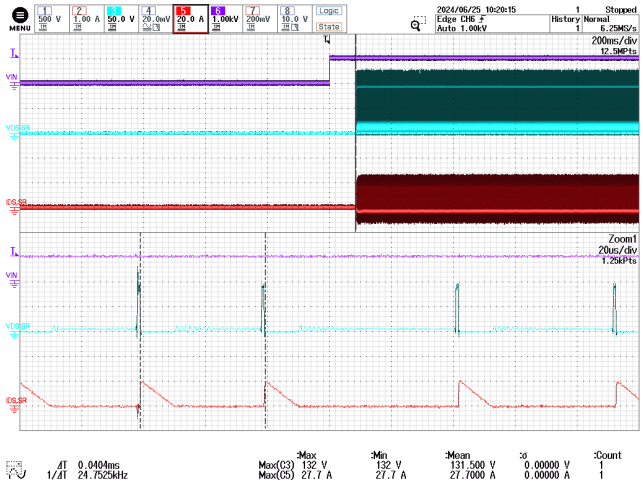


Figure 62 – SR FET Drain Voltage and Current.
1000 VDC, 4 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.1.3.3 24 W Peak Output Power

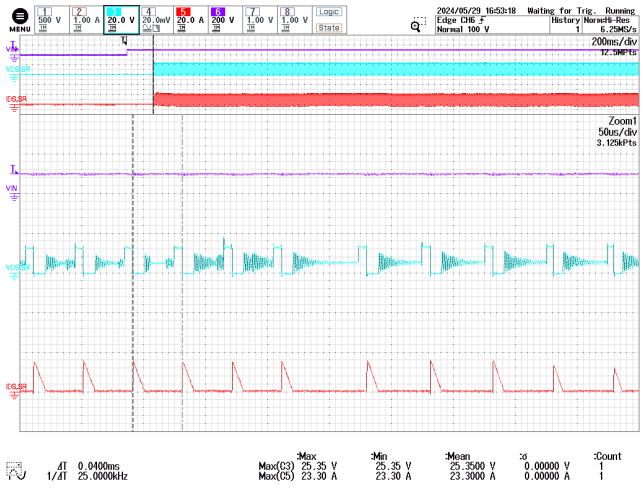


Figure 63 – SR FET Drain Voltage and Current.
100 VDC, 6 Ω Load.
CH3: $V_{DS,SR}$, 20 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

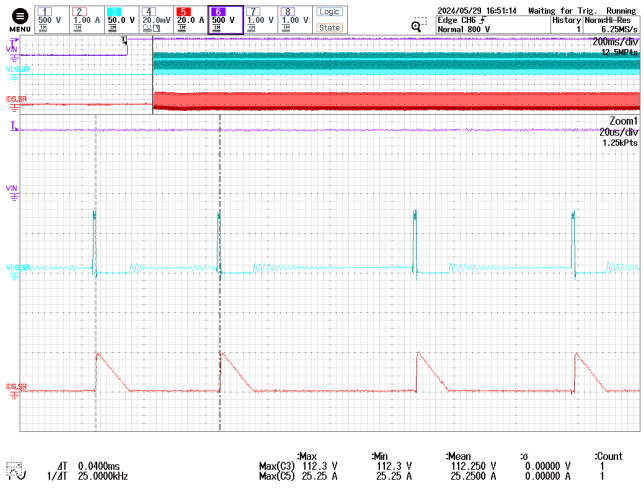


Figure 64 – SR FET Drain Voltage and Current.
800 VDC, 6 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

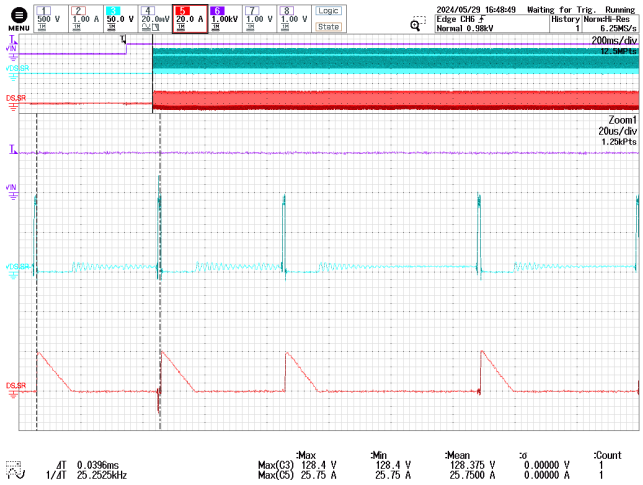


Figure 65 – SR FET Drain Voltage and Current.
1000 VDC, 6 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.1.4 Output Voltage and Current at 85 °C Ambient[21]

12.1.4.1 18 W Continuous Output Power

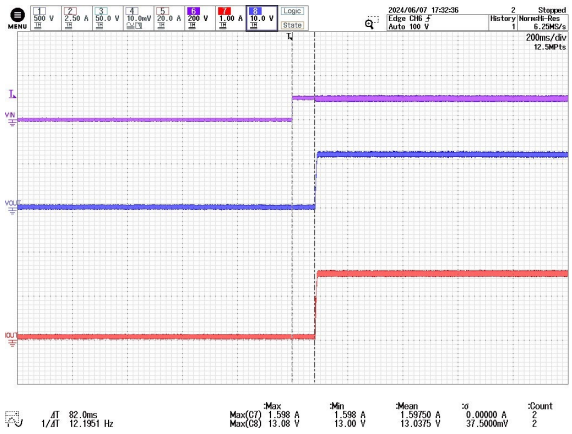


Figure 66 – Output Voltage and Current.
100 VDC, 8 Ω Load.
CH6: V_{IN}, 200 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

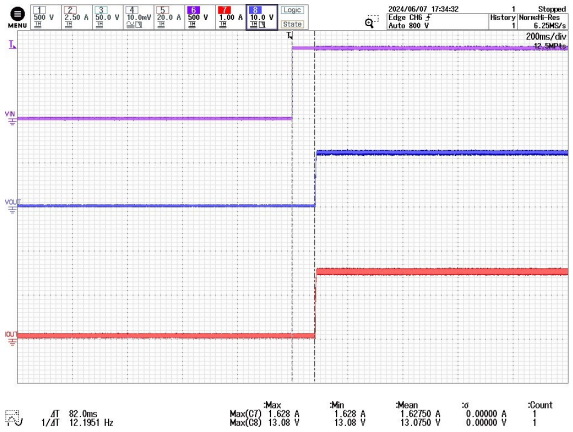


Figure 67 – Output Voltage and Current.
800 VDC, 8 Ω Load.
CH6: V_{IN}, 500 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

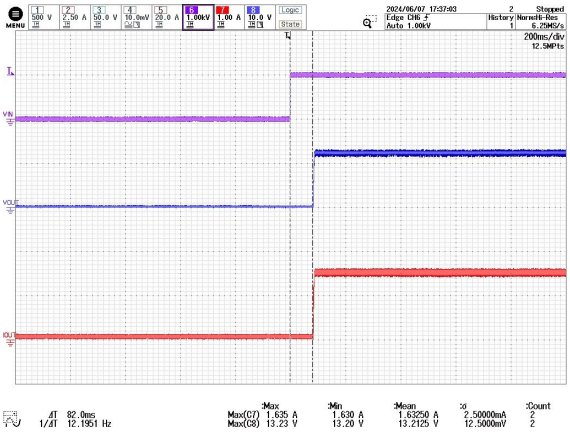


Figure 68 – Output Voltage and Current.
1000 VDC, 8 Ω Load.
CH6: V_{IN}, 1000 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

[21] Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.

12.1.4.2 36 W Peak Output Power

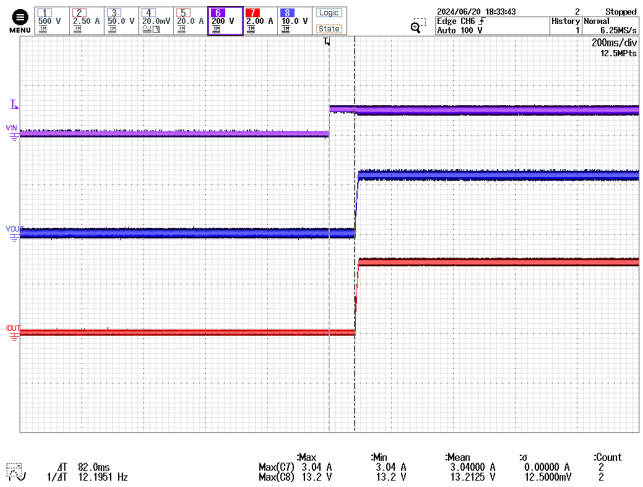


Figure 69 – Output Voltage and Current.
100 VDC, 4 Ω Load.
CH6: V_{IN}, 200 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 2 A / div.
Time: 200 ms / div.

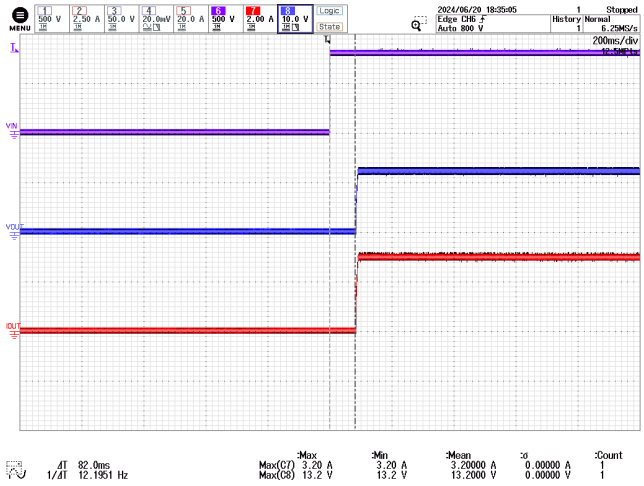


Figure 70 – Output Voltage and Current.
800 VDC, 4 Ω Load.
CH6: V_{IN}, 500 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 2 A / div.
Time: 200 ms / div.

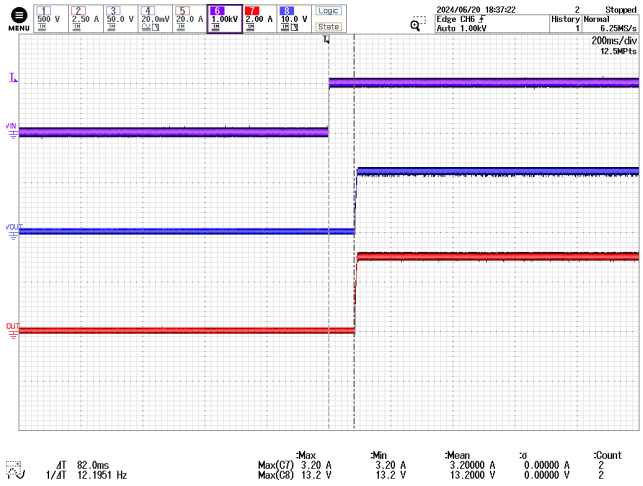


Figure 71 – Output Voltage and Current.
1000 VDC, 4 Ω Load.
CH6: V_{IN}, 1000 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 2 A / div.
Time: 200 ms / div.

12.1.4.3 24 W Peak Output Power

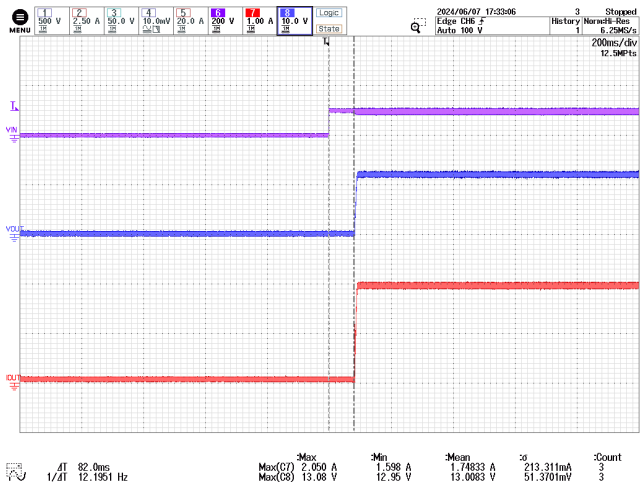


Figure 72 – Output Voltage and Current.
100 VDC, 6 Ω Load.
CH6: V_{IN}, 200 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

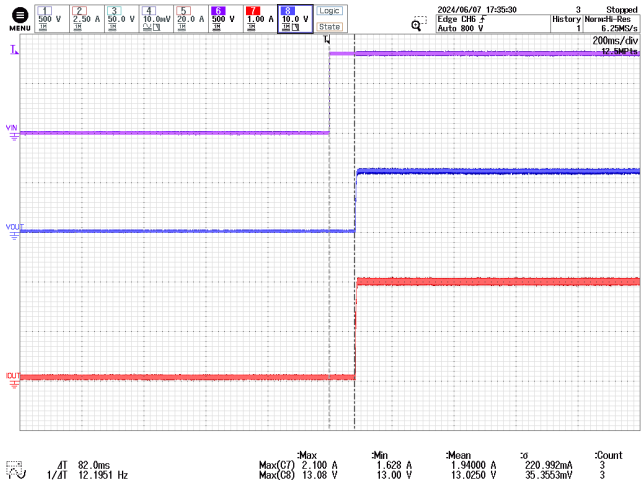


Figure 73 – Output Voltage and Current.
800 VDC, 6 Ω Load.
CH6: V_{IN}, 500 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

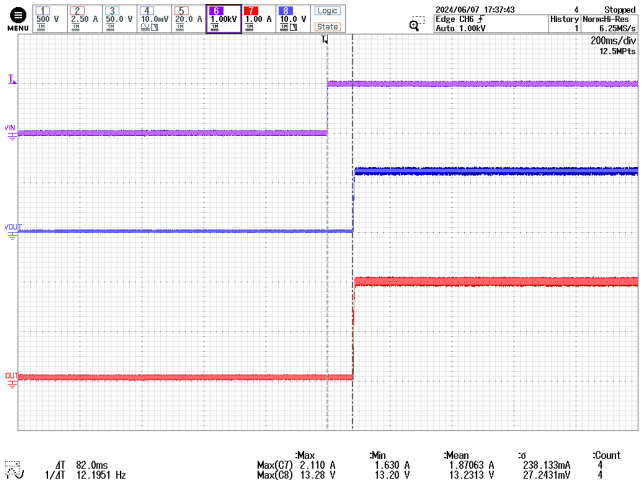


Figure 74 – Output Voltage and Current.
1000 VDC, 6 Ω Load.
CH6: V_{IN}, 1000 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

12.1.5 InnoSwitch3-AQ Drain Voltage and Current at 85 °C Ambient[22,23]

12.1.5.1 18 W Continuous Output Power

Figure 75 – INN3949FQ Drain Voltage and Current.
100 VDC, 8 Ω Load.
CH1: $V_{DS,INNO}$, 200 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

Figure 76 – INN3949FQ Drain Voltage and Current.
800 VDC, 8 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

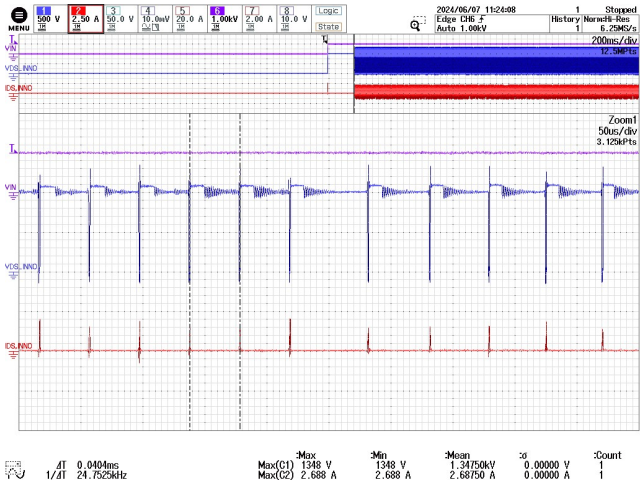


Figure 77 – INN3949FQ Drain Voltage and Current.
1000 VDC, 8 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH3: V_{IN}, 1000 V / div.
Time: 200 ms / div.

[22] The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[23] Current waveforms were measured using a Rogowski coil.

12.1.5.2 36 W Peak Output Power

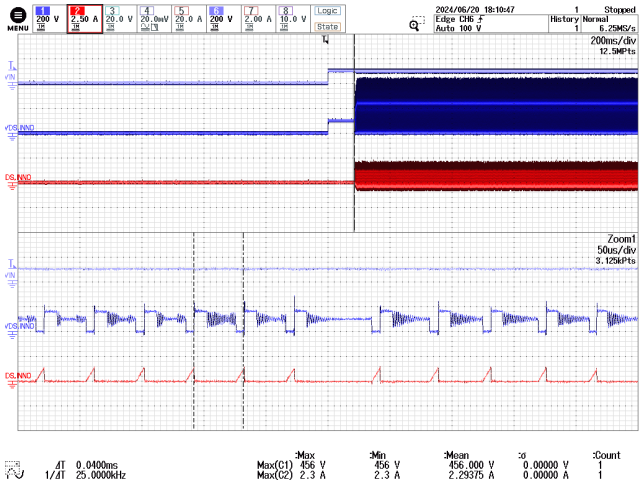


Figure 78 – INN3949FQ Drain Voltage and Current.
100 VDC, 4 Ω Load.
CH1: $V_{DS,INNO}$, 200 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

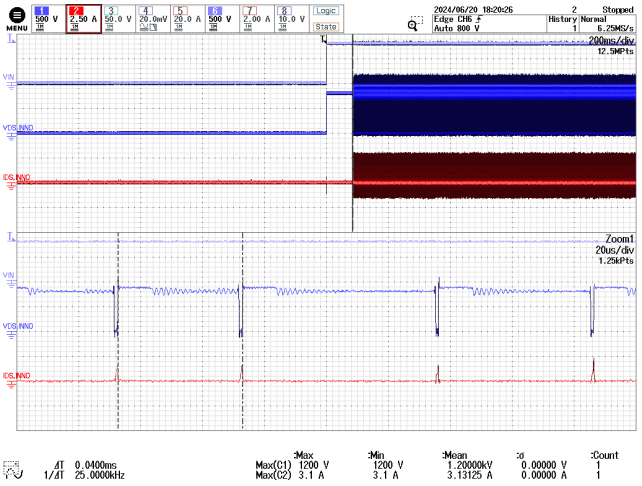


Figure 79 – INN3949FQ Drain Voltage and Current.
800 VDC, 4 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

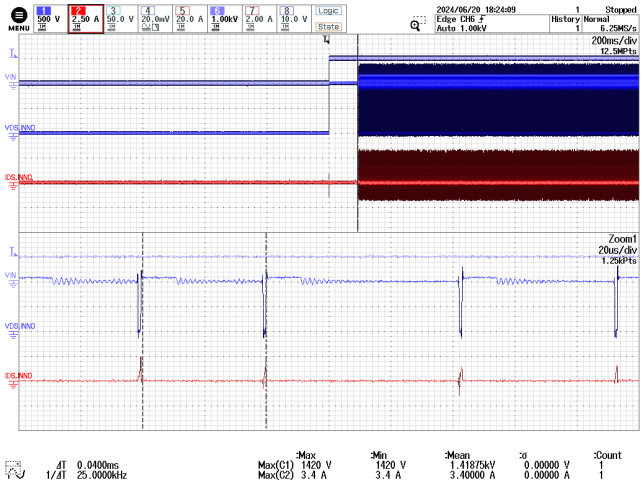


Figure 80 – INN3949FQ Drain Voltage and Current.
1000 VDC, 4 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.1.5.3 24 W Peak Output Power

Figure 81 – INN3949FQ Drain Voltage and Current.
100 VDC, 6 Ω Load.
CH1: $V_{DS,INNO}$, 200 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

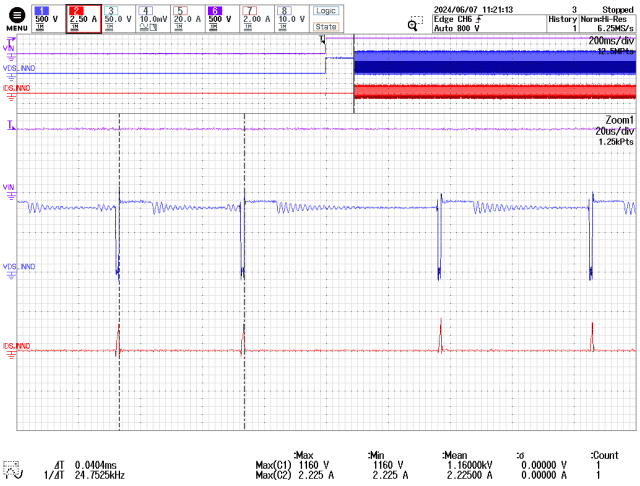


Figure 82 – INN3949FQ Drain Voltage and Current.
800 VDC, 6 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

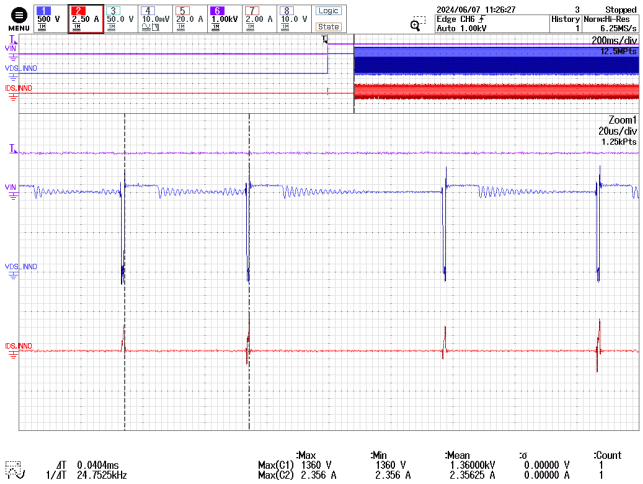


Figure 83 – INN3949FQ Drain Voltage and Current.
1000 VDC, 6 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.1.6 SR FET Drain Voltage and Current at 85 °C Ambient[24,25]

12.1.6.1 18 W Continuous Output Power

Figure 84 – SR FET Drain Voltage and Current.
100 VDC, 8 Ω Load.
CH3: $V_{DS,SR}$, 20 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

Figure 85 – SR FET Drain Voltage and Current.
800 VDC, 8 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

Figure 86 – SR FET Drain Voltage and Current.
1000 VDC, 8 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

[24] The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[25] Current waveforms were measured using a Rogowski coil.

12.1.6.2 36 W Peak Output Power

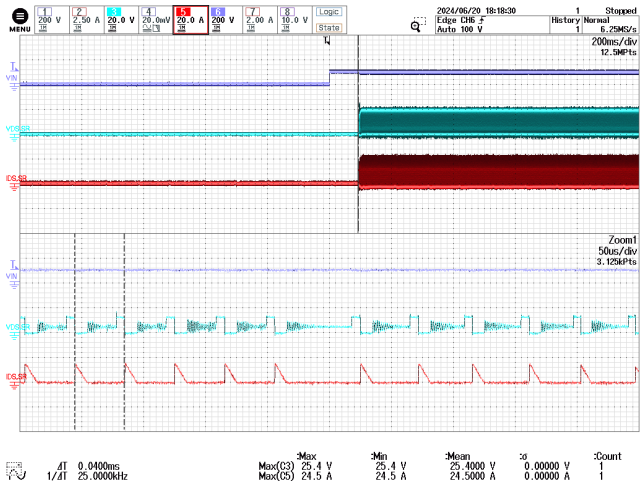


Figure 87 – SR FET Drain Voltage and Current.
100 VDC, 4 Ω Load.
CH3: $V_{DS,SR}$, 20 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

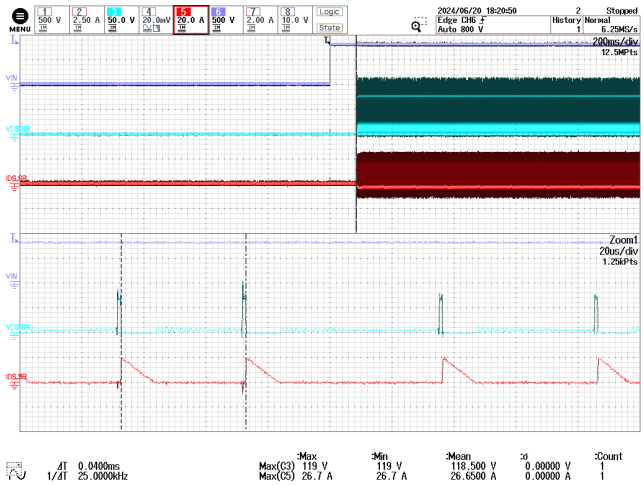


Figure 88 – SR FET Drain Voltage and Current.
800 VDC, 4 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

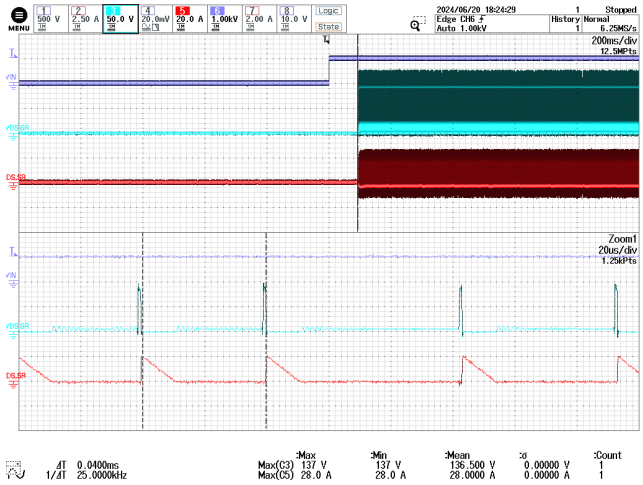


Figure 89 – SR FET Drain Voltage and Current.
1000 VDC, 4 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.1.6.3 24 W Peak Output Power

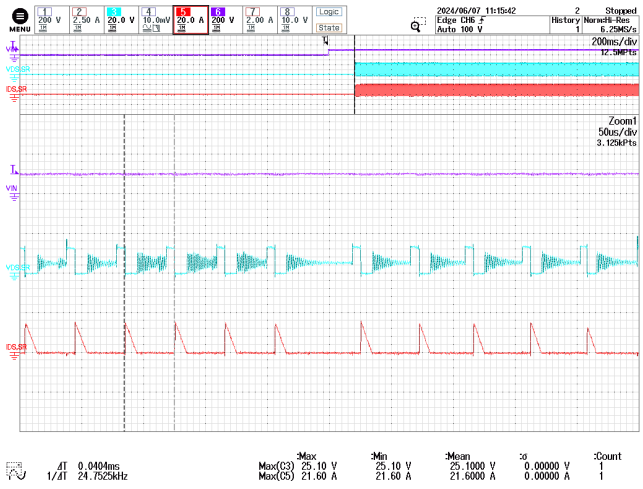


Figure 90 – SR FET Drain Voltage and Current.
100 VDC, 6 Ω Load.
CH3: $V_{DS,SR}$, 20 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

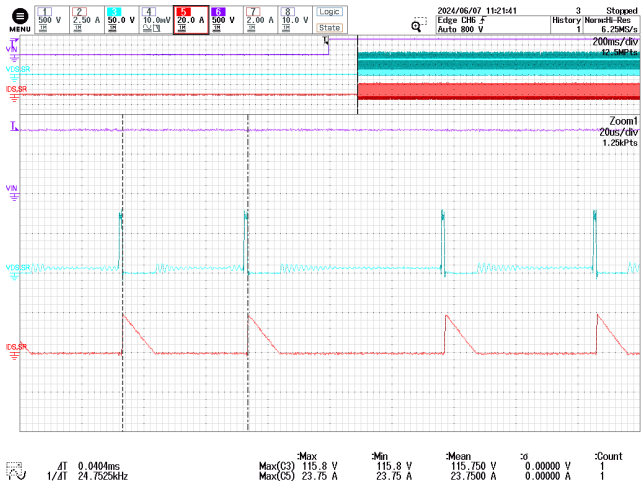


Figure 91 – SR FET Drain Voltage and Current.
800 VDC, 6 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

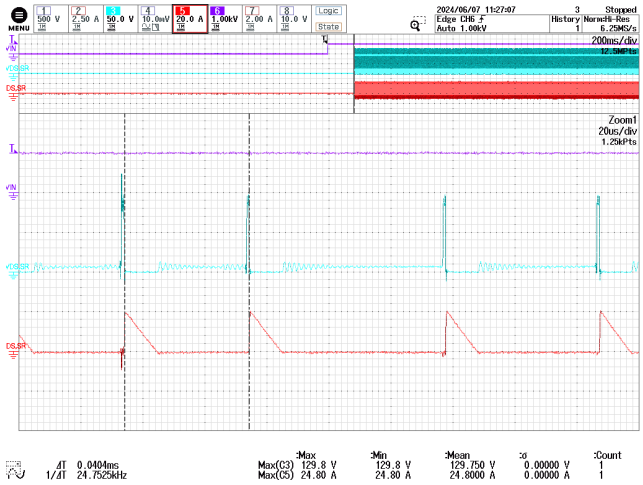


Figure 92 – SR FET Drain Voltage and Current.
1000 VDC, 6 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.1.7 Output Voltage and Current at -40 °C Ambient[26]

12.1.7.1 18 W Continuous Output Power

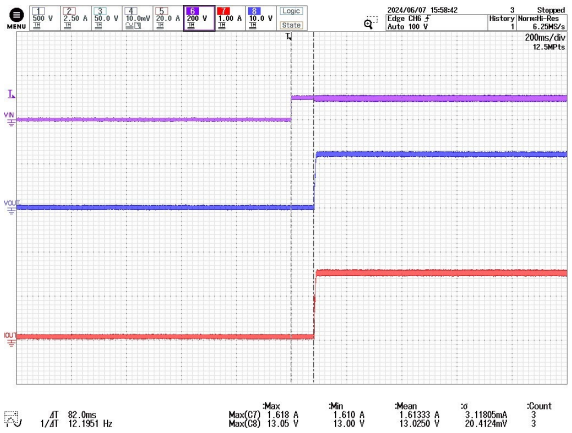


Figure 93 – Output Voltage and Current.
100 VDC, 8 Ω Load.
CH6: V_{IN}, 200 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

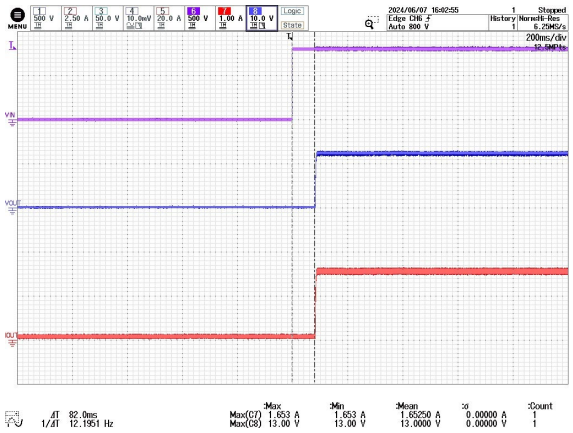


Figure 94 – Output Voltage and Current.
800 VDC, 8 Ω Load.
CH6: V_{IN}, 500 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

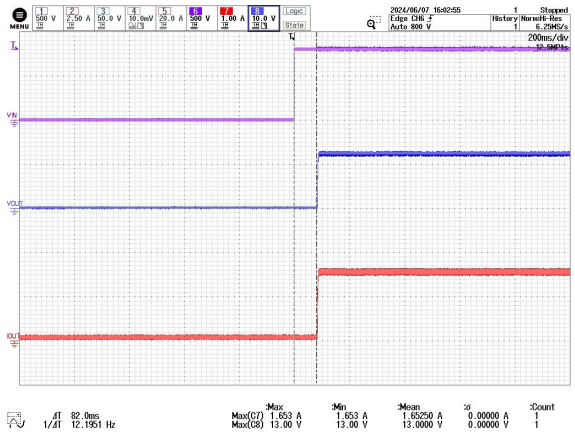


Figure 95 – Output Voltage and Current.
1000 VDC, 8 Ω Load.
CH6: V_{IN}, 1000 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

[26] Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.

12.1.7.2 36 W Peak Output Power

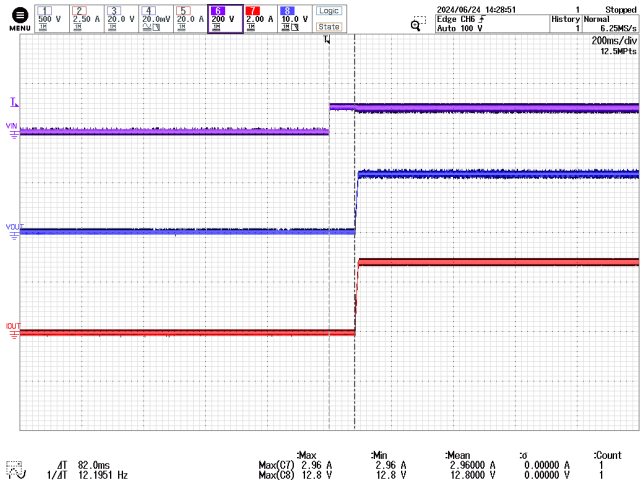


Figure 96 – Output Voltage and Current.
100 VDC, 4 Ω Load.
CH6: V_{IN}, 200 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 2 A / div.
Time: 200 ms / div.

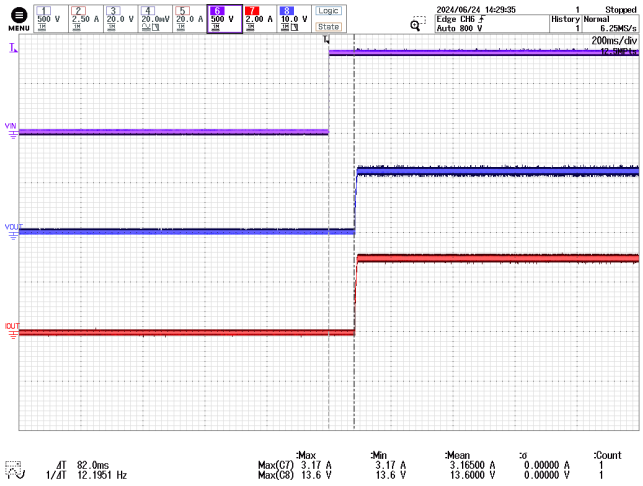


Figure 97 – Output Voltage and Current.
800 VDC, 4 Ω Load.
CH6: V_{IN}, 500 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 2 A / div.
Time: 200 ms / div.

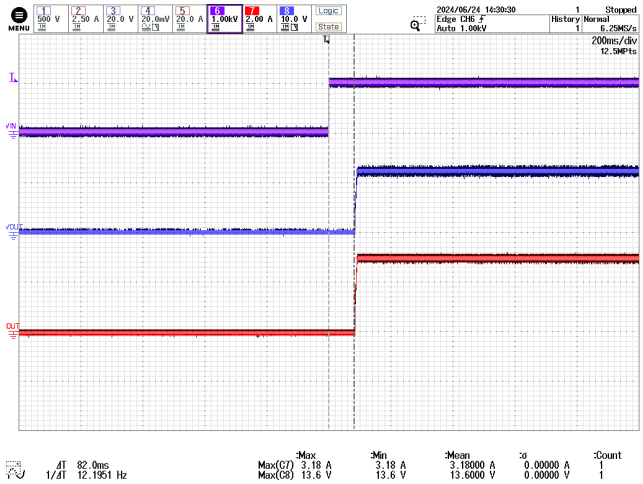


Figure 98 – Output Voltage and Current.
1000 VDC, 4 Ω Load.
CH6: V_{IN}, 1000 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 2 A / div.
Time: 200 ms / div.

12.1.7.3 24 W Peak Output Power

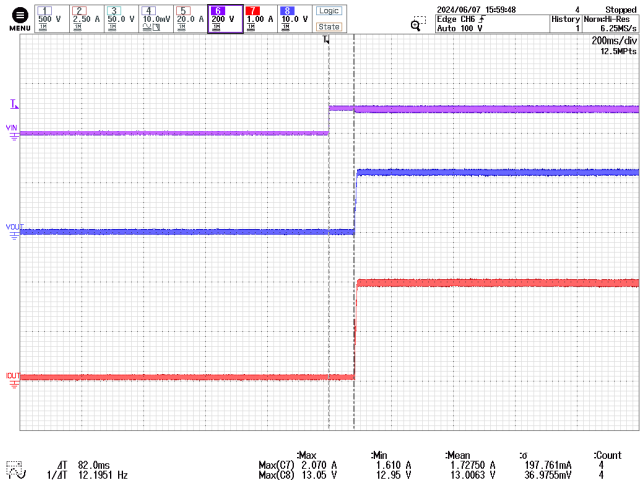


Figure 99 – Output Voltage and Current.
100 VDC, 6 Ω Load.
CH6: V_{IN}, 200 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

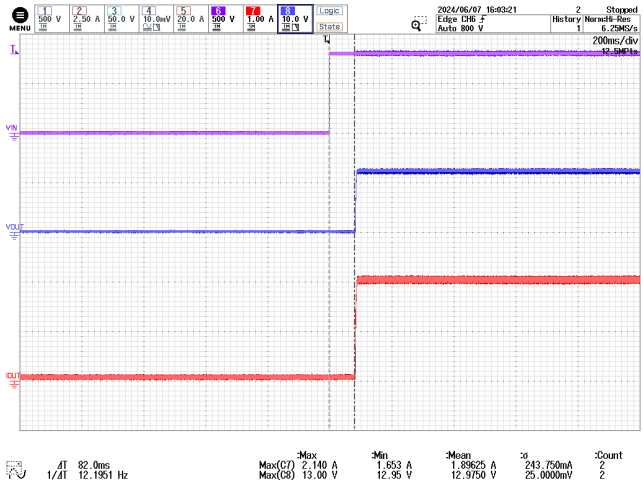


Figure 100 – Output Voltage and Current.
800 VDC, 6 Ω Load.
CH6: V_{IN}, 500 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

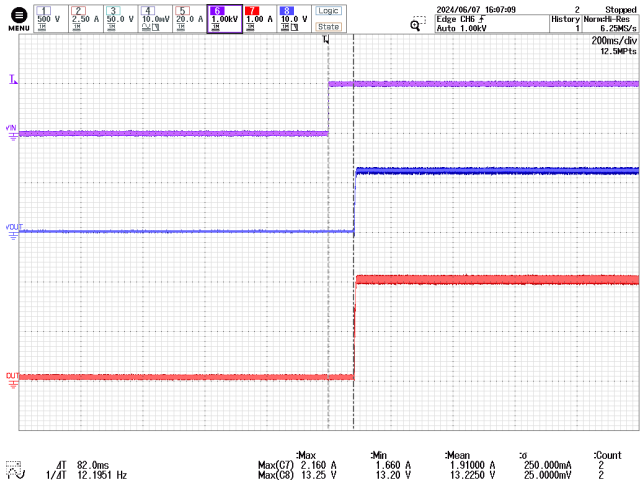


Figure 101 – Output Voltage and Current.
1000 VDC, 6 Ω Load.
CH6: V_{IN}, 1000 V / div.
CH8: V_{OUT}, 10 V / div.
CH7: I_{OUT}, 1 A / div.
Time: 200 ms / div.

12.1.8 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient[27,28]

12.1.8.1 18 W Continuous Output Power

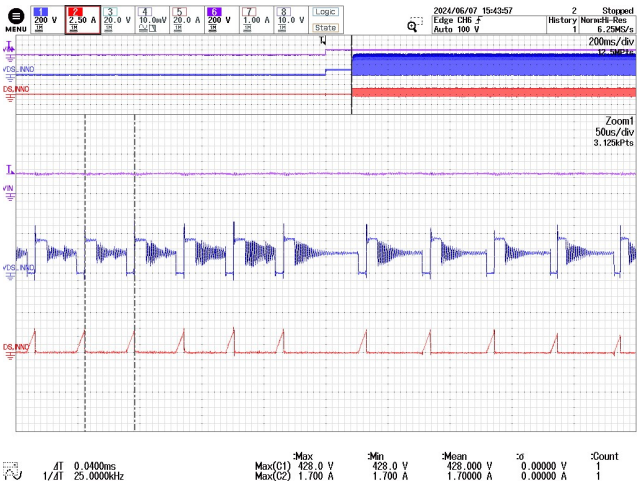


Figure 102 – INN3949FQ Drain Voltage and Current.
100 VDC, 8 Ω Load.
CH1: $V_{DS,INNO}$, 200 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

Figure 103 – INN3949FQ Drain Voltage and Current.
800 VDC, 8 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

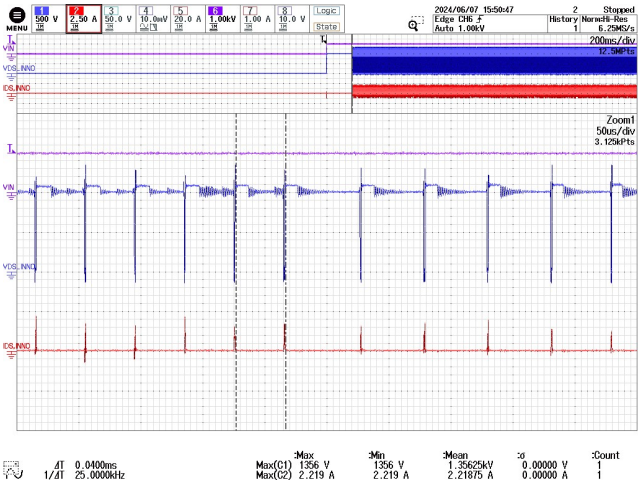


Figure 104 – INN3949FQ Drain Voltage and Current.
1000 VDC, 8 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH3: V_{IN}, 1000 V / div.
Time: 200 ms / div.

[27] The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[28] Current waveforms were measured using a Rogowski coil.

12.1.8.2 36 W Peak Output Power

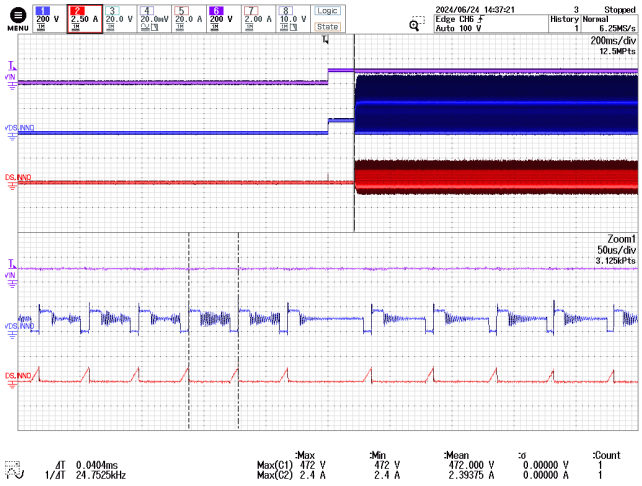


Figure 105 – INN3949FQ Drain Voltage and Current.
100 VDC, 4 Ω Load.
CH1: $V_{DS,INNO}$, 200 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

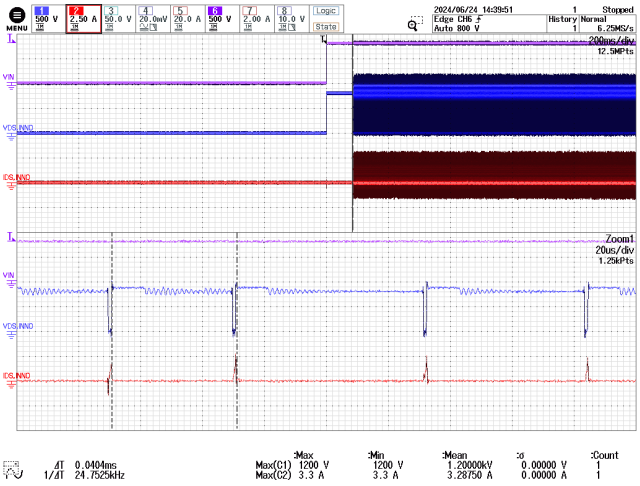


Figure 106 – INN3949FQ Drain Voltage and Current.
800 VDC, 4 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

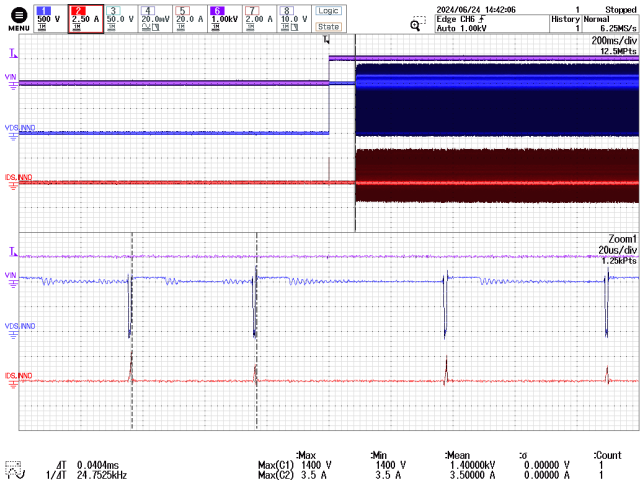


Figure 107 – INN3949FQ Drain Voltage and Current.
1000 VDC, 4 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH3: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.1.8.3 24 W Peak Output Power

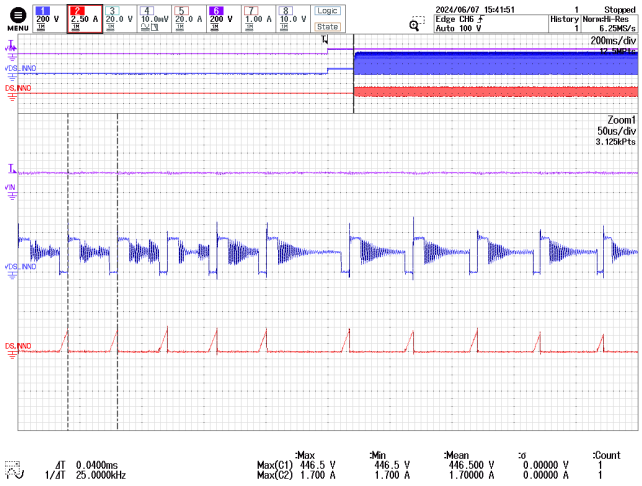


Figure 108 – INN3949FQ Drain Voltage and Current.
100 VDC, 6 Ω Load.
CH1: $V_{DS,INNO}$, 200 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

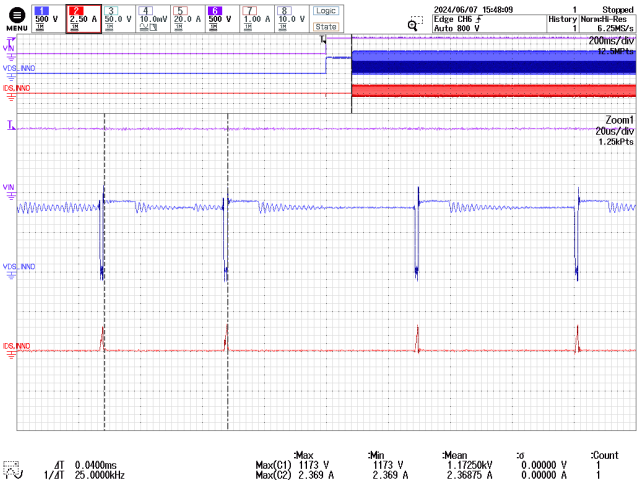


Figure 109 – INN3949FQ Drain Voltage and Current.
800 VDC, 6 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

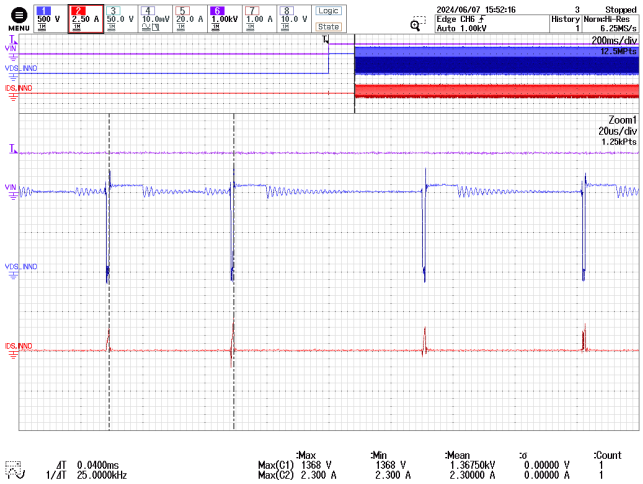


Figure 110 – INN3949FQ Drain Voltage and Current.
1000 VDC, 6 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{DS,INNO}$, 2.50 A / div.
CH3: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.1.9 SR FET Drain Voltage and Current at -40 °C Ambient[29,30]

12.1.9.1 18 W Continuous Output Power

Figure 111 – SR FET Drain Voltage and Current.
100 VDC, 8 Ω Load.
CH3: $V_{DS,SR}$, 20 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

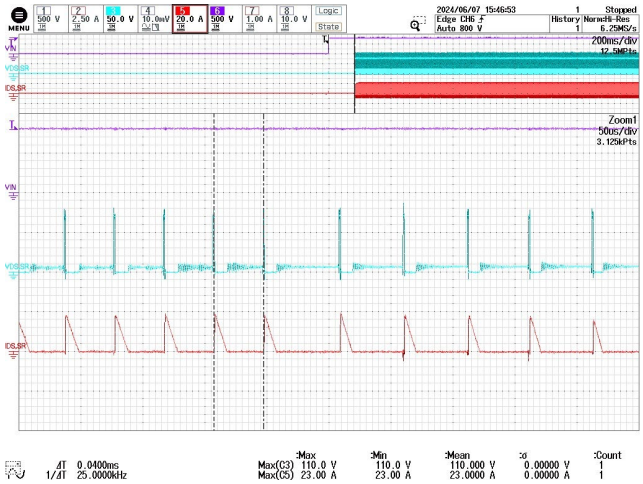


Figure 112 – SR FET Drain Voltage and Current.
800 VDC, 8 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

Figure 113 – SR FET Drain Voltage and Current.
1000 VDC, 8 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

[29] The time between when V_{IN} turned on and the InnoSwitch3 starts switching was due to the "Wait and Listen" period of the InnoSwitch3.
[30] Current waveforms were measured using a Rogowski coil.

12.1.9.2 36 W Peak Output Power

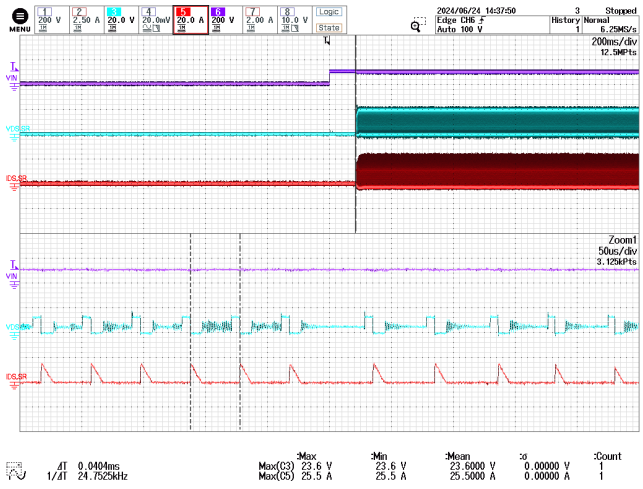


Figure 114 – SR FET Drain Voltage and Current.
100 VDC, 4 Ω Load.
CH3: $V_{DS,SR}$, 20 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

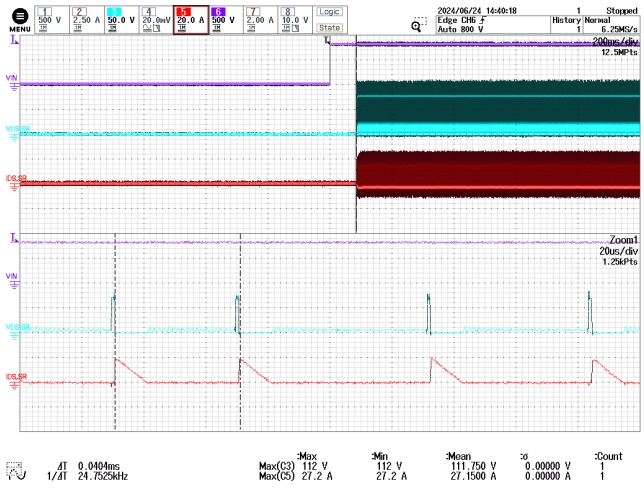


Figure 115 – SR FET Drain Voltage and Current.
800 VDC, 4 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

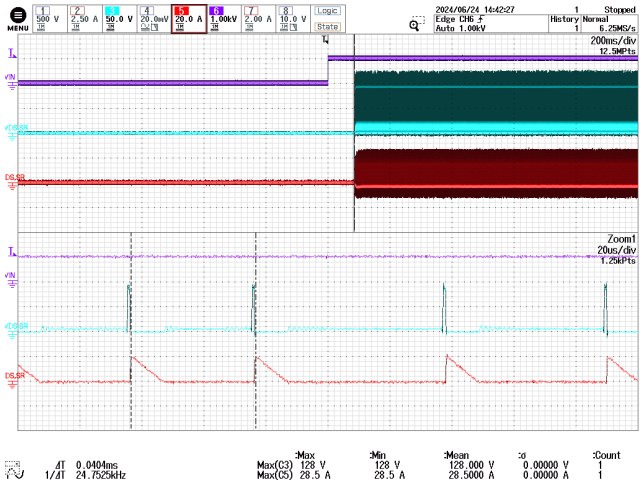


Figure 116 – SR FET Drain Voltage and Current.
1000 VDC, 4 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.1.9.3 24 W Peak Output Power

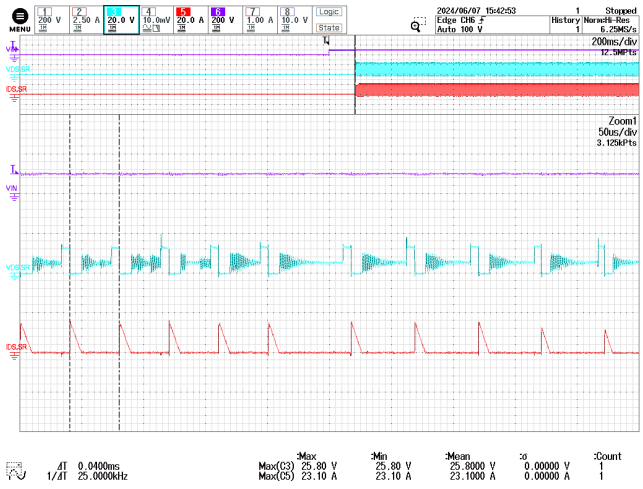


Figure 117 – SR FET Drain Voltage and Current.
100 VDC, 6 Ω Load.
CH3: $V_{DS,SR}$, 20 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 200 V / div.
Time: 200 ms / div.

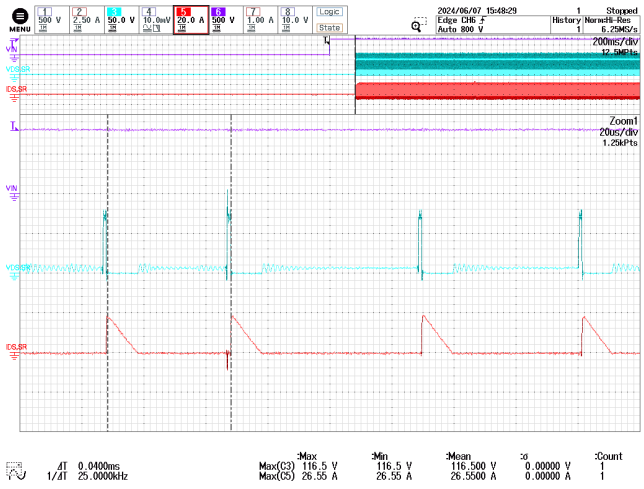


Figure 118 – SR FET Drain Voltage and Current.
800 VDC, 6 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 500 V / div.
Time: 200 ms / div.

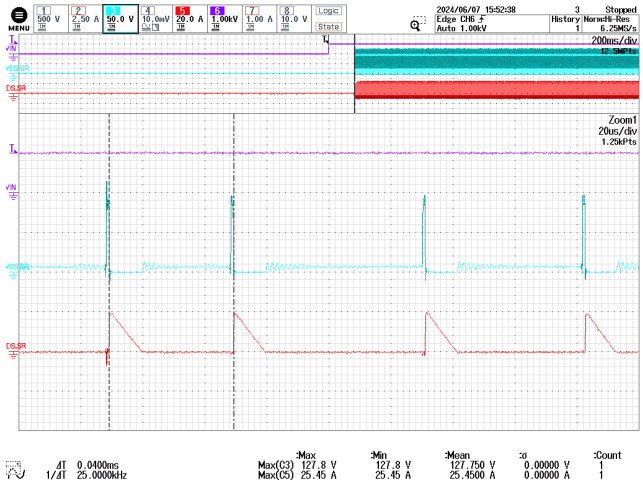


Figure 119 – SR FET Drain Voltage and Current.
1000 VDC, 6 Ω Load.
CH3: $V_{DS,SR}$, 50 V / div.
CH5: $I_{D,SR}$, 20 A / div.
CH6: V_{IN}, 1000 V / div.
Time: 200 ms / div.

12.2 Steady-State Waveforms

12.2.1 Switching Waveforms at 25 °C Ambient

12.2.1.1 Normal Operation Component Stresses at 18 W Continuous Output[31,32]

Steady-State Switching Waveforms 25 °C Ambient, 1.5 A, 18 W Continuous Output Power						
Input	**INN3949FQ**			**SR FET**		
V_{IN} (VDC)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**
100	1.57	443	26.1	23.4	24.9	16.6
800	1.66	1110	65.3	23.9	109	72.7
1000	1.69	1330	78.2	24.9	127	84.7

Table 10 – Summary of Voltage Stress on Critical Components at 25 °C Ambient, 18 W Output Power.

[31] SR FET current is the sum of Q1 and Q2 currents.
[32] SR FET voltage was taken from Q1.

12.2.1.1.1 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient

Figure 120 – INN3949FQ Drain Voltage and Current.
100 VDC, 1.5 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
Time: 10 μs / div.

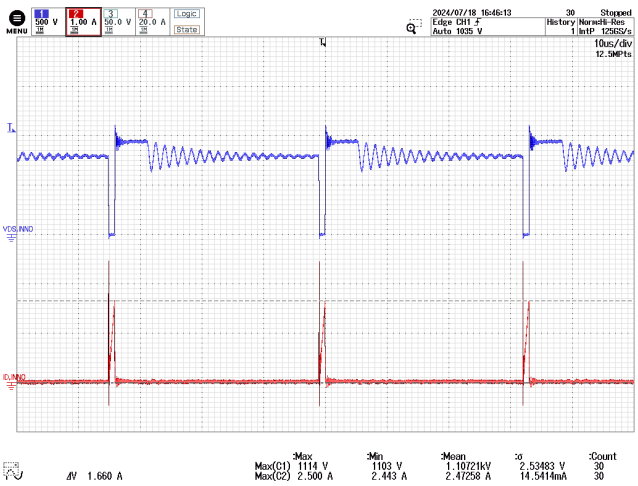


Figure 121 – INN3949FQ Drain Voltage and Current.
800 VDC, 1.5 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
Time: 10 μs / div.

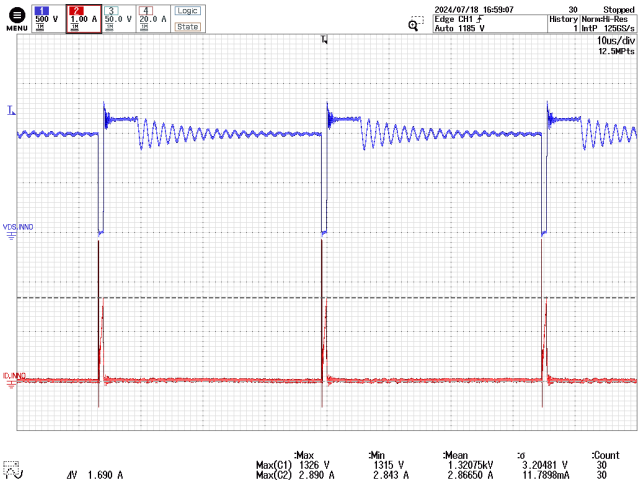


Figure 122 – INN3949FQ Drain Voltage and Current.
1000 VDC, 1.5 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
Time: 10 μs / div.

12.2.1.1.2 SR FET Drain Voltage and Current at 25 °C Ambient

Figure 123 – SR FET Drain Voltage and Current.
100 VDC, 1.5 A Load, 25 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

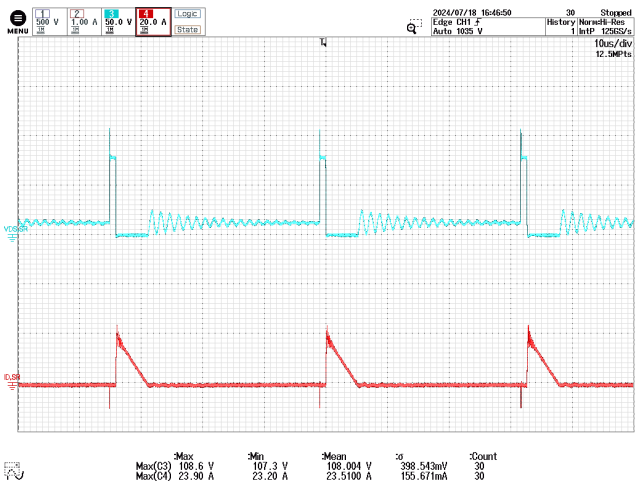


Figure 124 – SR FET Drain Voltage and Current.
800 VDC, 1.5 A Load, 25 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

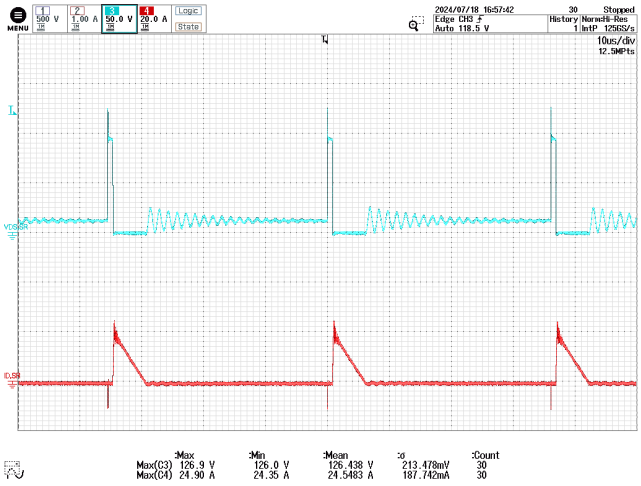


Figure 125 – SR FET Drain Voltage and Current.
1000 VDC, 1.5 A Load, 25 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

12.2.1.1.3 Short-Circuit Response at 25 °C Ambient

The unit was tested by applying an output short-circuit during normal operation and then removing the short-circuit to determine whether the unit would recover and operate normally. During a short-circuit, the expected response is for the unit to enter auto-restart (AR) mode and attempt to recover every 1.7 to 2.11 seconds.

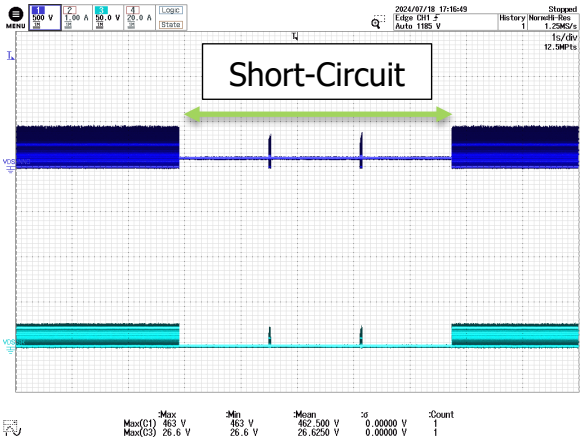


Figure 126 – INN3949FQ and SR FET Drain Voltage. 100 VDC, 1.5 A-Short-1.5 A, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH3: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

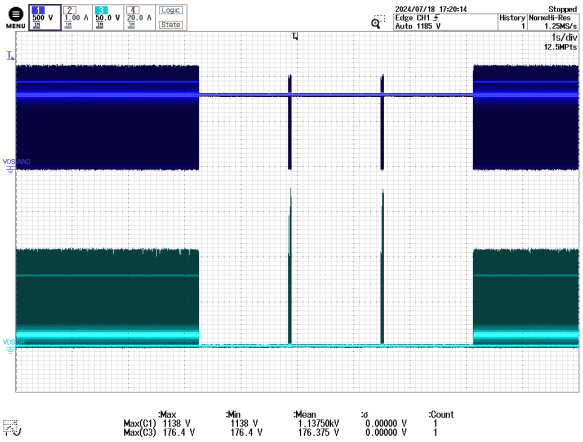


Figure 127 – INN3949FQ and SR FET Drain Voltage. 800 VDC, 1.5 A-Short-1.5 A, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH3: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

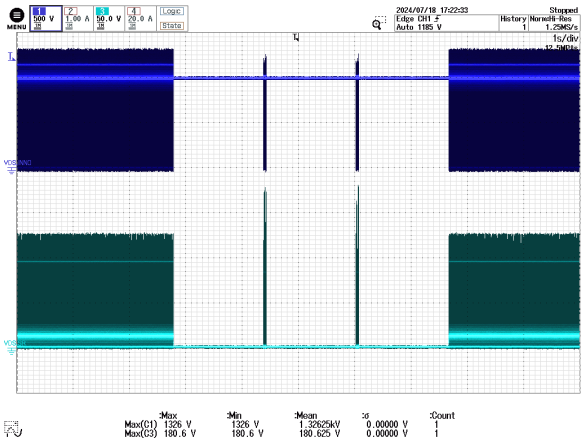


Figure 128 – INN3949FQ and SR FET Drain Voltage. 1000 VDC, 1.5 A-Short-1.5 A, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH3: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

12.2.1.2 Normal Operation Component Stresses at 36 W Peak Output Power[33,34]

Steady-State Switching Waveforms 25 °C Ambient, 3 A, 36 W Peak Output Power						
Input	**INN3949FQ**			**SR FET**		
V_{IN} (VDC)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**
100	1.74	490	28.8	26	23.5	15.7
800	1.94	1170	68.8	27.5	108	72.0
1000	1.96	1380	81.2	28.1	127	84.7

Table 11 – Summary of Voltage Stress on Critical Components at 25 °C Ambient, 36 W Peak Output Power.

[33] SR FET current is the sum of Q1 and Q2 currents.
[34] SR FET voltage was taken from Q1.

12.2.1.2.1 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient

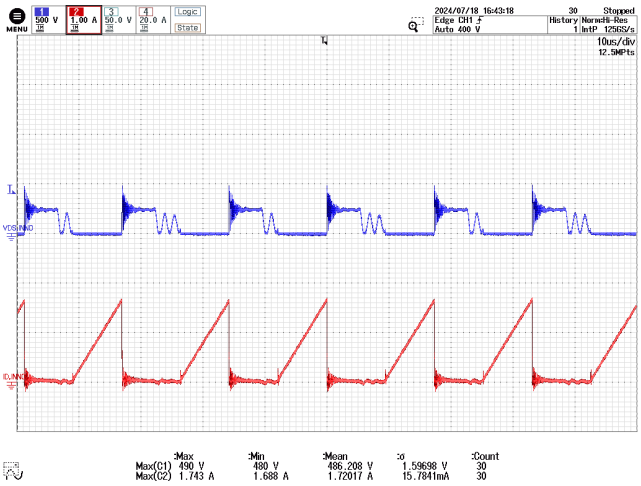


Figure 129 – INN3949FQ Drain Voltage and Current.
100 VDC, 3 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
Time: 10 μs / div.

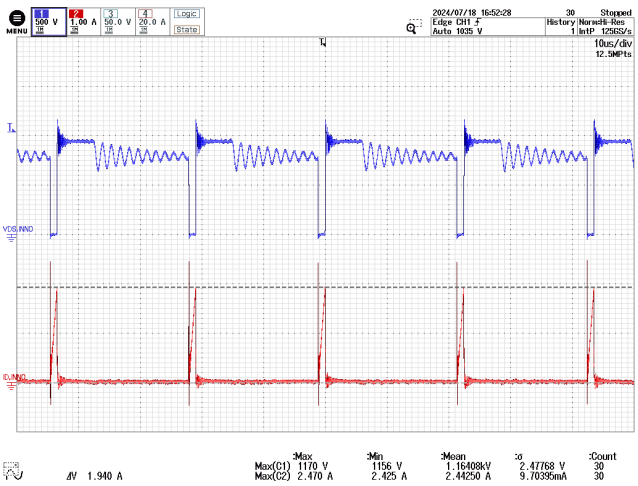


Figure 130 – INN3949FQ Drain Voltage and Current.
800 VDC, 3 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
Time: 10 μs / div.

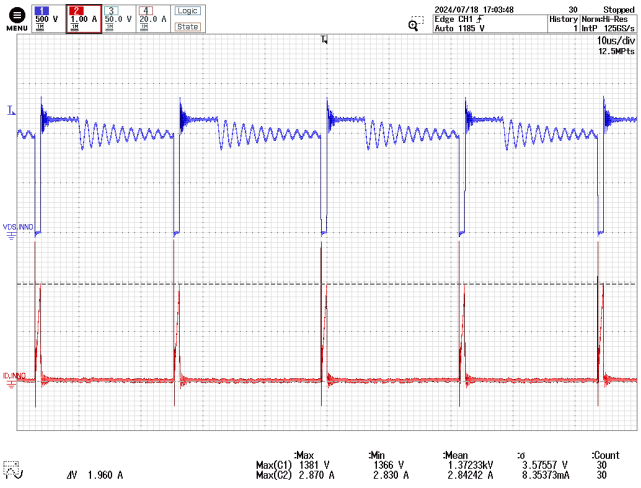


Figure 131 – INN3949FQ Drain Voltage and Current.
1000 VDC, 3 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
Time: 10 μs / div.

12.2.1.2.2 SR FET Drain Voltage and Current at 25 °C Ambient

Figure 132 – SR FET Drain Voltage and Current.
100 VDC, 3 A Load, 25 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 µs / div.

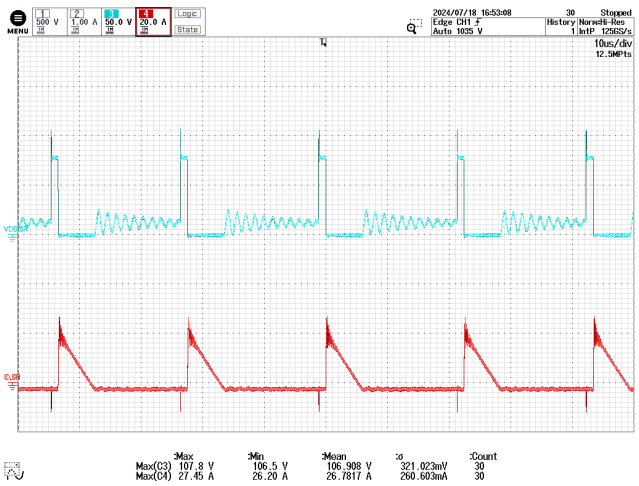


Figure 133 – SR FET Drain Voltage and Current.
800 VDC, 3 A Load, 25 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 µs / div.

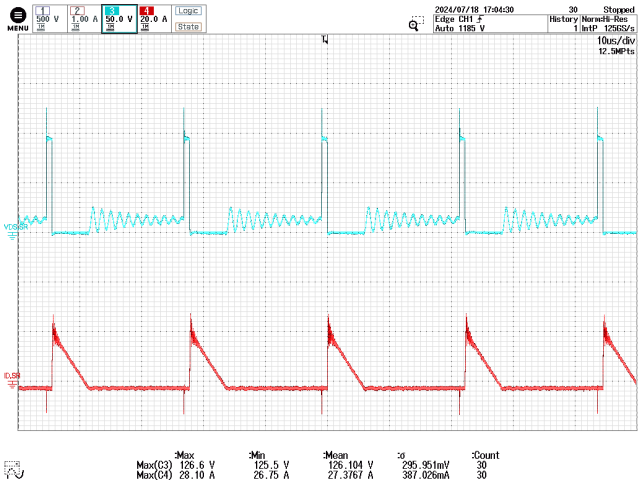


Figure 134 – SR FET Drain Voltage and Current.
1000 VDC, 3 A Load, 25 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 µs / div.

12.2.1.2.3 Short-Circuit Response at 25 °C Ambient

The unit was tested by applying an output short-circuit during normal operation and then removing the short-circuit to determine whether the unit would recover and operate normally. During a short-circuit, the expected response is for the unit to enter auto-restart (AR) mode and attempt to recover every 1.7 to 2.11 seconds.

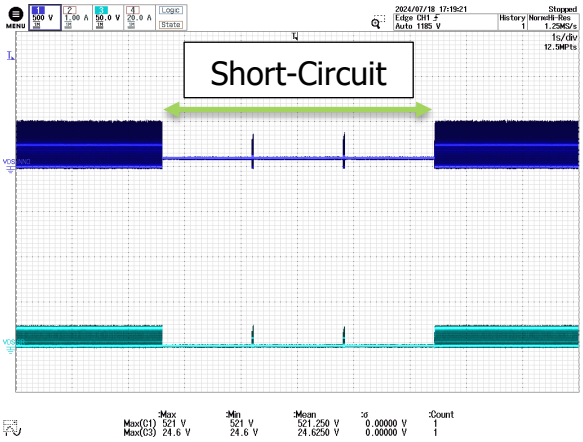


Figure 135 – INN3949FQ and SR FET Drain Voltage.
100 VDC, 3 A-Short-3 A, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH3: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

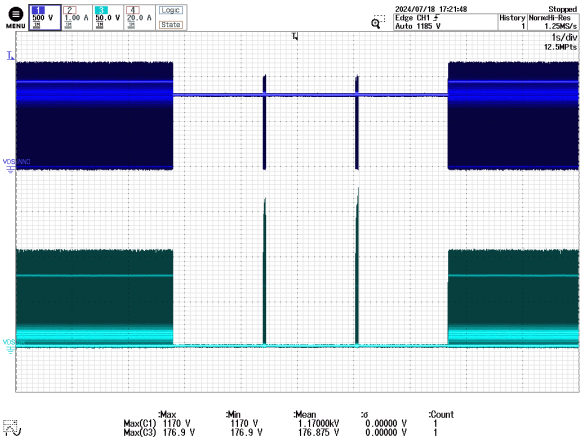


Figure 136 – INN3949FQ and SR FET Drain Voltage.
800 VDC, 3 A-Short-3 A, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH3: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

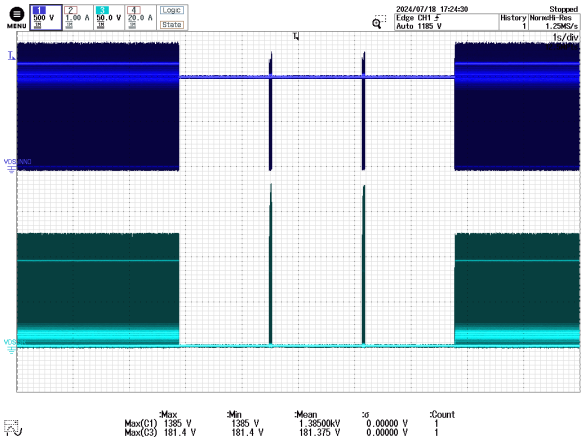


Figure 137 – INN3949FQ and SR FET Drain Voltage.
1000 VDC, 3 A-Short-3 A, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH3: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

12.2.1.3 Normal Operation Component Stresses at 24 W Peak Output Power[35,36]

Steady-State Switching Waveforms 25 °C Ambient, 2 A, 24 W Peak Output Power						
Input	**INN3949FQ**			**SR FET**		
V_{IN} (VDC)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**
100	1.66	463	27.2	24.4	24.9	16.6
800	1.79	1140	67.1	25.8	108	72.0
1000	1.81	1340	78.8	26.6	127	84.7

Table 12 – Summary of Voltage Stress on Critical Components at 25 °C Ambient, 24 W Peak Output Power.

[35] SR FET current is the sum of Q1 and Q2 currents.
[36] SR FET voltage was taken from Q1.

12.2.1.3.1 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient

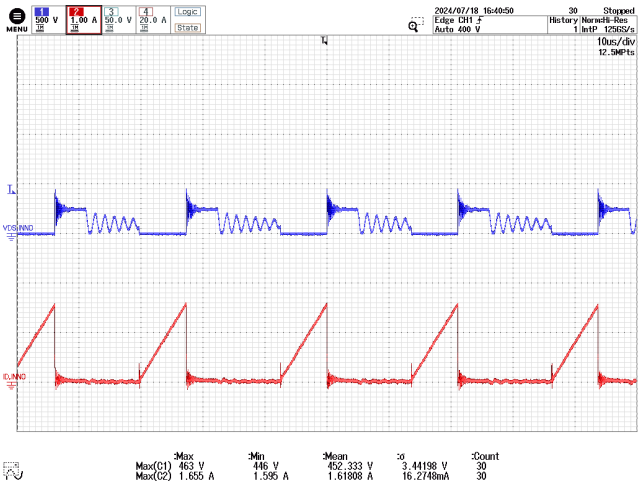


Figure 138 – INN3949FQ Drain Voltage and Current.
100 VDC, 2 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
Time: 10 μs / div.

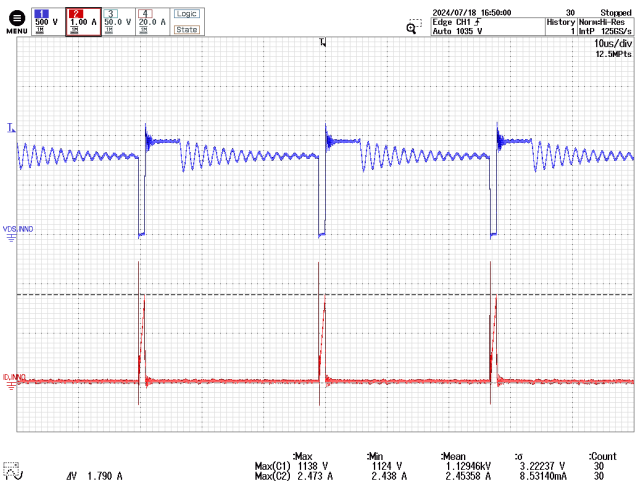


Figure 139 – INN3949FQ Drain Voltage and Current.
800 VDC, 2 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
Time: 10 μs / div.

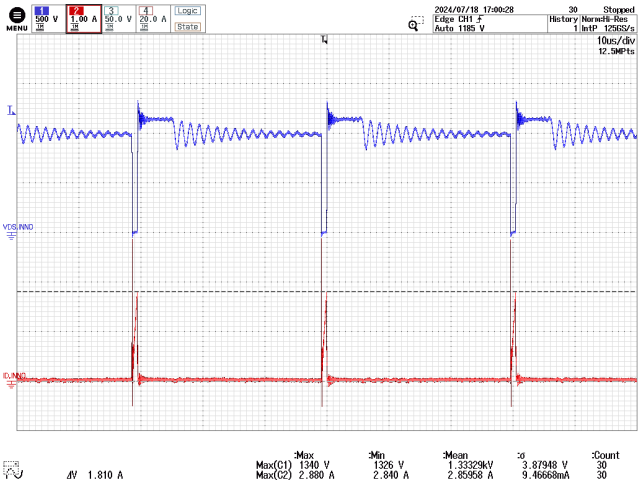


Figure 140 – INN3949FQ Drain Voltage and Current.
1000 VDC, 2 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 1.00 A / div.
Time: 10 μs / div.

12.2.1.3.2 SR FET Drain Voltage and Current at 25 °C Ambient

Figure 141 – SR FET Drain Voltage and Current.
100 VDC, 2 A Load, 25 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 µs / div.

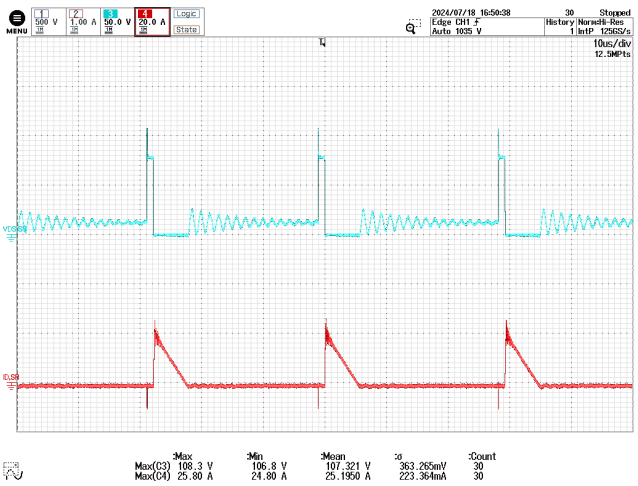


Figure 142 – SR FET Drain Voltage and Current.
800 VDC, 2 A Load, 25 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 µs / div.

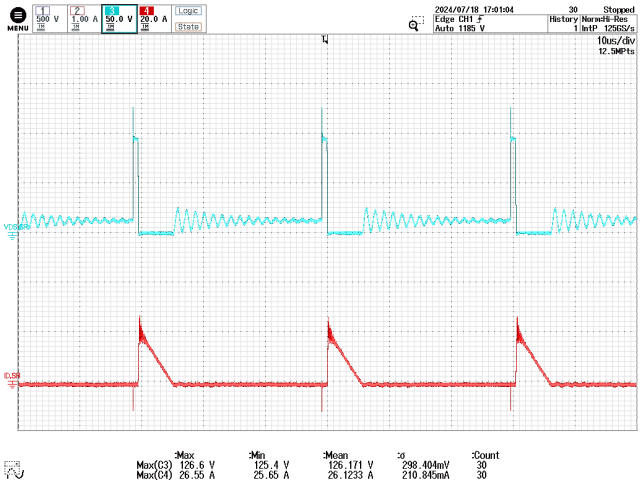


Figure 143 – SR FET Drain Voltage and Current.
1000 VDC, 2 A Load, 25 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 µs / div.

12.2.1.3.3 Short-Circuit Response at 25 °C Ambient

The unit was tested by applying an output short-circuit during normal operation and then removing the short-circuit to determine whether the unit would recover and operate normally. During a short-circuit, the expected response is for the unit to enter auto-restart (AR) mode and attempt to recover every 1.7 to 2.11 seconds.

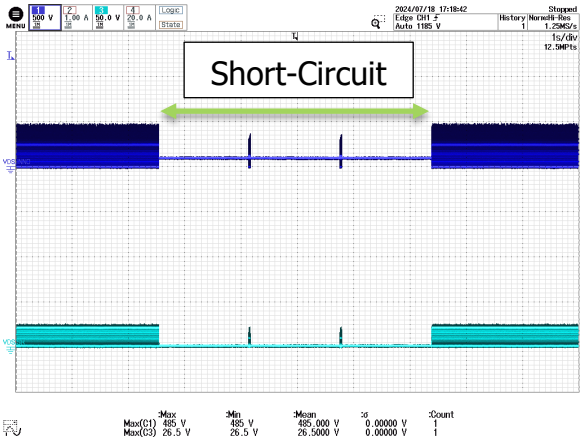


Figure 144 – INN3949FQ and SR FET Drain Voltage.
100 VDC, 2 A-Short-2 A, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH3: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

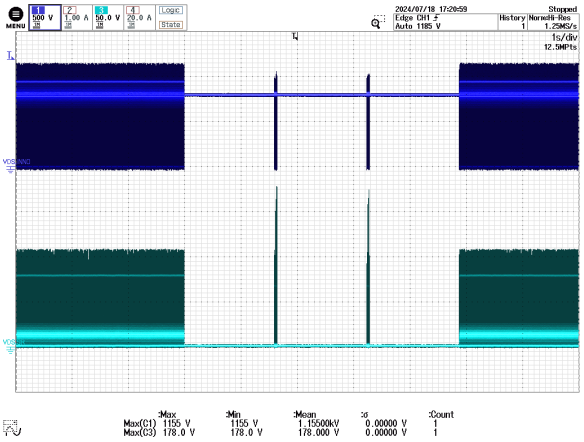


Figure 145 – INN3949FQ and SR FET Drain Voltage.
800 VDC, 2 A-Short-2 A, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH3: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

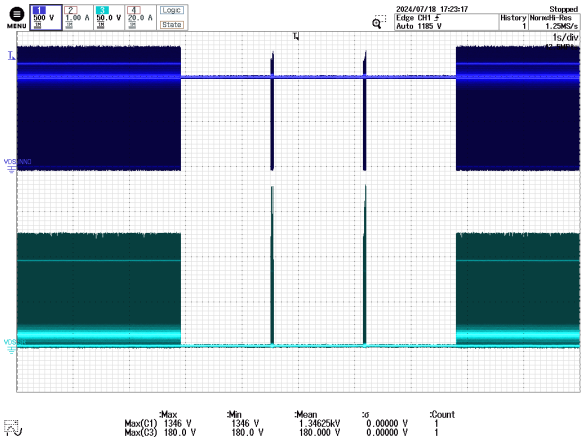


Figure 146 – INN3949FQ and SR FET Drain Voltage.
1000 VDC, 2 A-Short-2 A, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH3: $V_{DS,SR}$, 50 V / div.
Time: 1 s / div.

12.2.2 Switching Waveforms at 85 °C Ambient

12.2.2.1 Normal Operation Component Stresses at 18 W Continuous Output [37,38]

Steady-State Switching Waveforms 85 °C Ambient, 1.5 A, 18 W Continuous Output Power						
Input	**INN3949FQ**			**SR FET**		
V_{IN} (VDC)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**
100	1.53	435	25.6	22.4	24.9	16.6
800	1.58	1110	65.3	23.5	109	72.7
1000	1.80	1330	78.2	24.4	130	86.7

Table 13 – Summary of Voltage Stress on Critical Components at 85 °C Ambient, 1.5 A Load, 18 W Output Power.

[37] SR FET current is the sum of Q1 and Q2 currents.
[38] SR FET voltage was taken from Q1.

12.2.2.1.1 InnoSwitch3-AQ Drain Voltage and Current at 85 °C Ambient

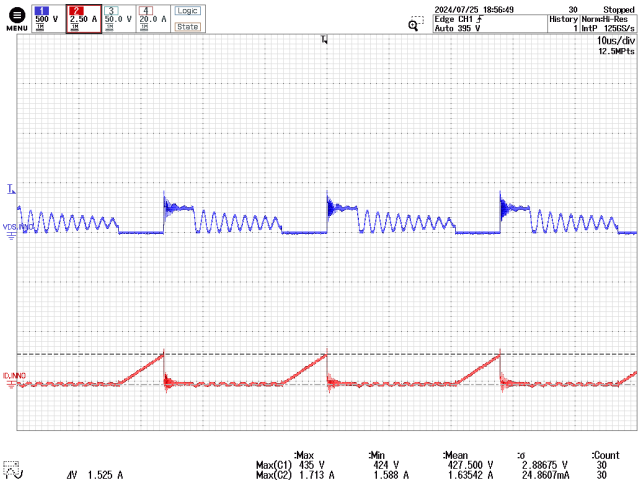


Figure 147 – INN3949FQ Drain Voltage and Current.
100 VDC, 1.5 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

Figure 148 – INN3949FQ Drain Voltage and Current.
800 VDC, 1.5 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

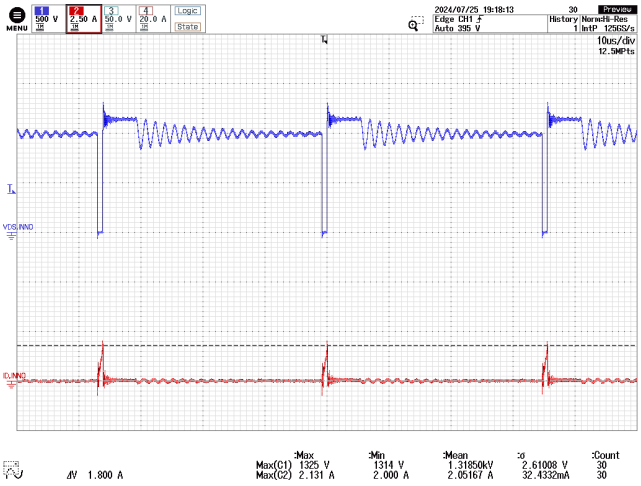


Figure 149 – INN3949FQ Drain Voltage and Current.
1000 VDC, 1.5 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

12.2.2.1.2 SR FET Drain Voltage and Current at 85 °C Ambient

Figure 150 – SR FET Drain Voltage and Current.
100 VDC, 1.5 A Load, 85 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

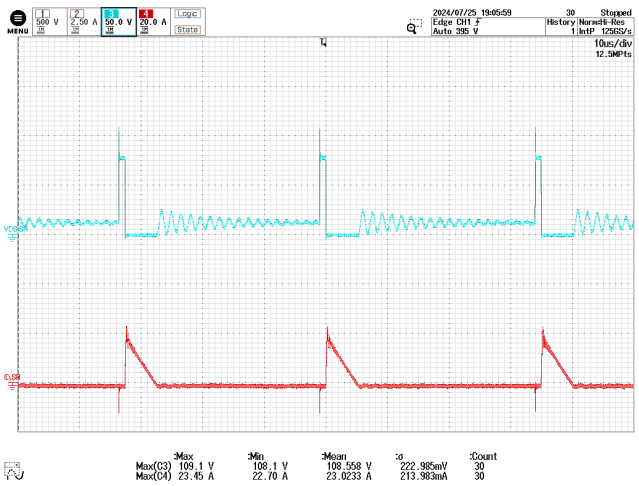


Figure 151 – SR FET Drain Voltage and Current.
800 VDC, 1.5 A Load, 85 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

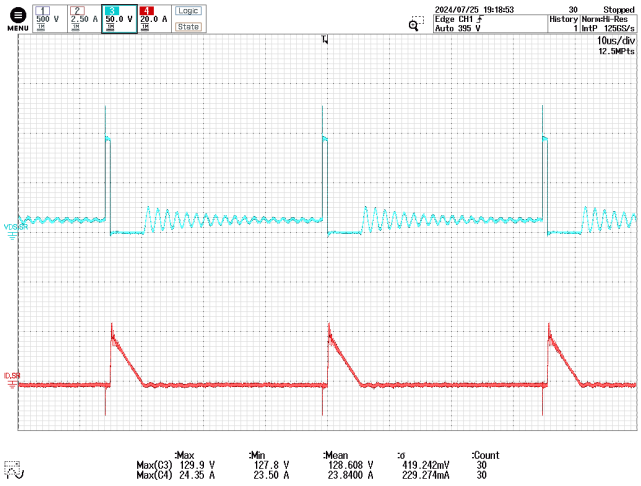


Figure 152 – SR FET Drain Voltage and Current.
1000 VDC, 1.5 A Load, 85 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

12.2.2.2 Normal Operation Component Stresses at 36 W Peak Output Power[39,40]

Steady-State Switching Waveforms 85 °C Ambient, 3 A, 36 W Peak Output Power						
Input	**INN3949FQ**			**SR FET**		
V_{IN} (VDC)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**
100	1.73	469	27.6	24.6	22.4	14.9
800	2.1	1280	75.3	31.0	109	72.7
1000	2.1	1460	85.9	32.2	128	85.3

Table 14 – Summary of Voltage Stress on Critical Components at 85 °C Ambient, 36 W Peak Output Power.

[39] SR FET current is the sum of Q1 and Q2 currents.
[40] SR FET voltage was taken from Q1.

12.2.2.2.1 InnoSwitch3-AQ Drain Voltage and Current at 85 °C Ambient

Figure 153 – INN3949FQ Drain Voltage and Current.
100 VDC, 3 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

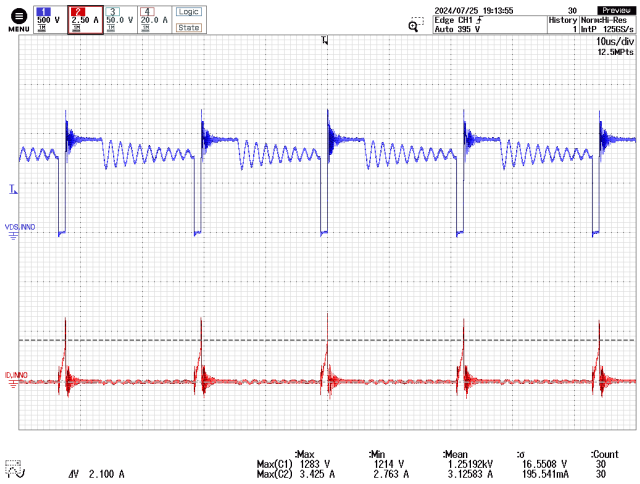


Figure 154 – INN3949FQ Drain Voltage and Current.
800 VDC, 3 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

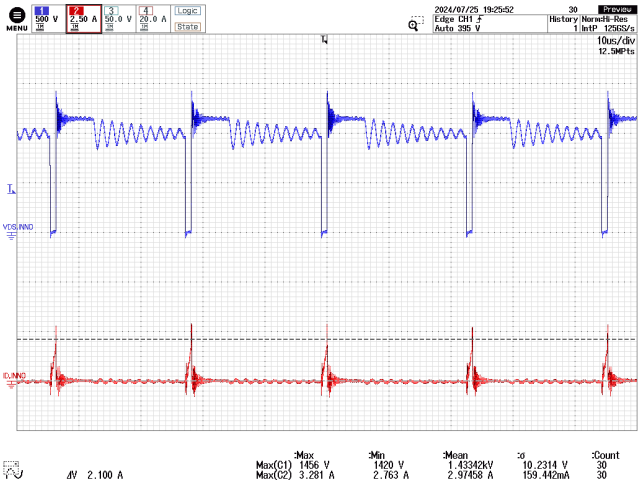


Figure 155 – INN3949FQ Drain Voltage and Current.
1000 VDC, 3 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

12.2.2.2.2 SR FET Drain Voltage and Current at 85 °C Ambient

Figure 156 – SR FET Drain Voltage and Current.
100 VDC, 3 A Load, 85 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

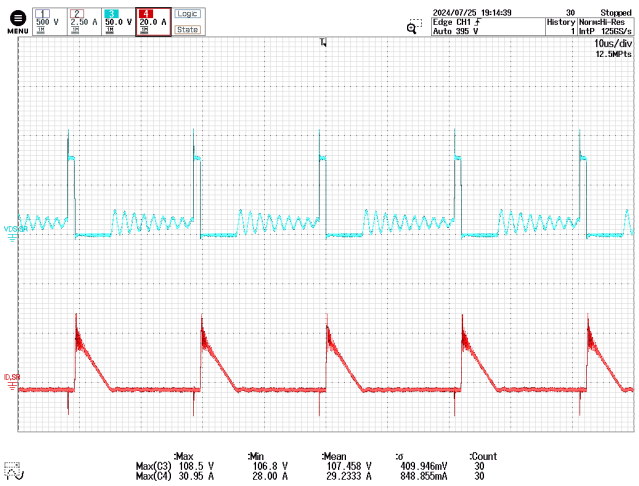


Figure 157 – SR FET Drain Voltage and Current.
800 VDC, 3 A Load, 85 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

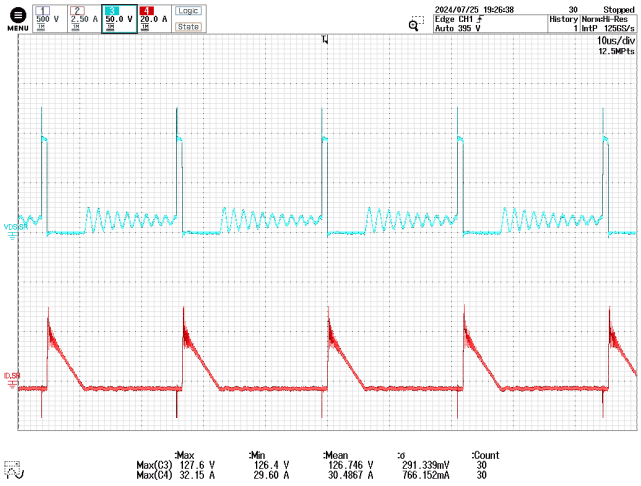


Figure 158 – SR FET Drain Voltage and Current.
1000 VDC, 3 A Load, 85 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

12.2.2.3 Normal Operation Component Stresses at 24 W Peak Output Power[41,42]

Steady-State Switching Waveforms 85 °C Ambient, 2 A, 24 W Peak Output Power						
Input	**INN3949FQ**			**SR FET**		
V_{IN} (VDC)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**
100	1.58	441	25.9	23.4	24.1	16.1
800	1.70	1140	67.1	25.6	108	72.0
1000	1.85	1350	79.4	26.7	129	86.0

Table 15 – Summary of Voltage Stress on Critical Components at 85 °C Ambient, 24 W Peak Output Power.

[41] SR FET current is the sum of Q1 and Q2 currents.
[42] SR FET voltage was taken from Q1.

12.2.2.3.1 InnoSwitch3-AQ Drain Voltage and Current at 85 °C Ambient

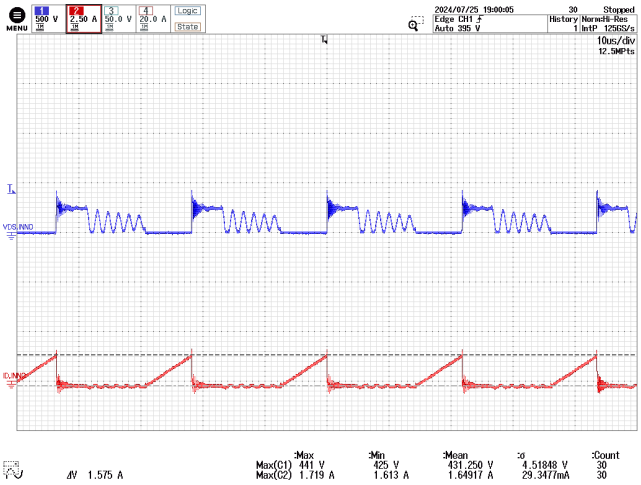


Figure 159 – INN3949FQ Drain Voltage and Current.
100 VDC, 2 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 μs / div.

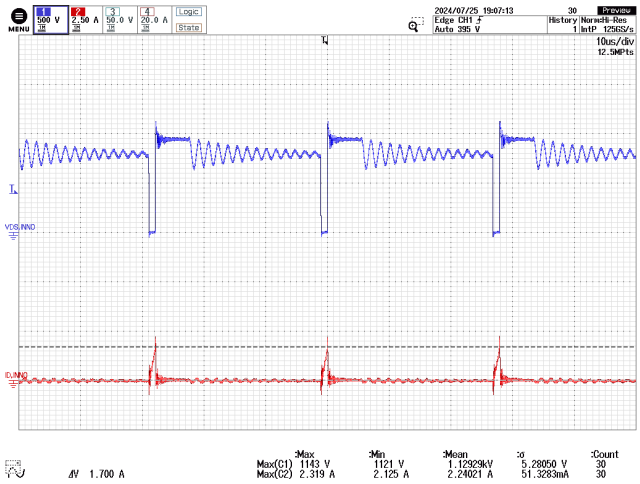


Figure 160 – INN3949FQ Drain Voltage and Current.
800 VDC, 2 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 μs / div.

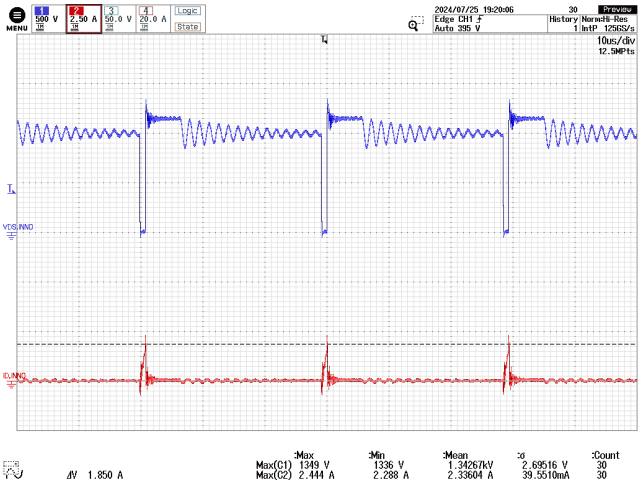


Figure 161 – INN3949FQ Drain Voltage and Current.
1000 VDC, 2 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 μs / div.

12.2.2.3.2 SR FET Drain Voltage and Current at 85 °C Ambient

Figure 162 – SR FET Drain Voltage and Current.
100 VDC, 2 A Load, 85 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 µs / div.

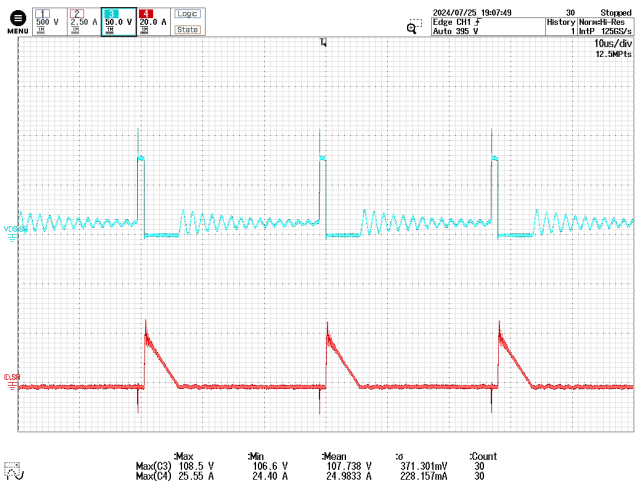


Figure 163 – SR FET Drain Voltage and Current.
800 VDC, 2 A Load, 85 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 µs / div.

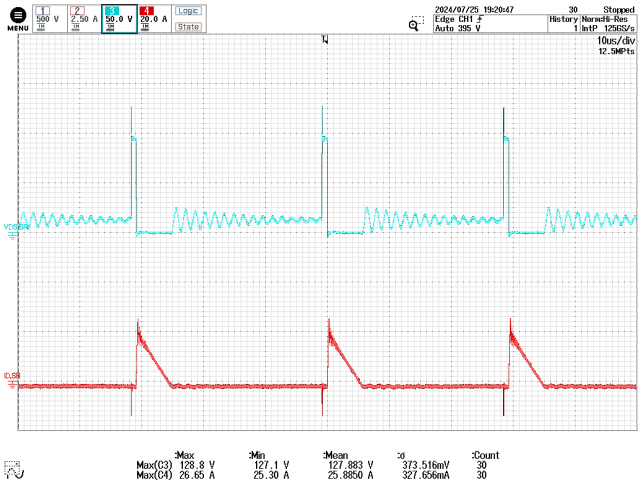


Figure 164 – SR FET Drain Voltage and Current.
1000 VDC, 2 A Load, 85 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 µs / div.

12.2.3 Switching Waveforms at -40 °C Ambient

12.2.3.1 Normal Operation Component Stresses at 18 W Continuous Output [43,44]

Steady-State Switching Waveforms -40 °C Ambient, 1.5 A, 18 W Continuous Output Power						
Input	**INN3949FQ**			**SR FET**		
V_{IN} (VDC)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**
100	1.60	480	28.2	23.8	24.9	16.6
800	1.63	1150	67.6	25.0	109	72.7
1000	1.65	1370	80.6	25.9	129	86.0

Table 16 – Summary of Voltage Stress on Critical Components at -40 °C Ambient, 1.5 A Load, 18 W Output Power.

[43] SR FET current is the sum of Q1 and Q2 currents.
[44] SR FET voltage was taken from Q1.

12.2.3.1.1 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient

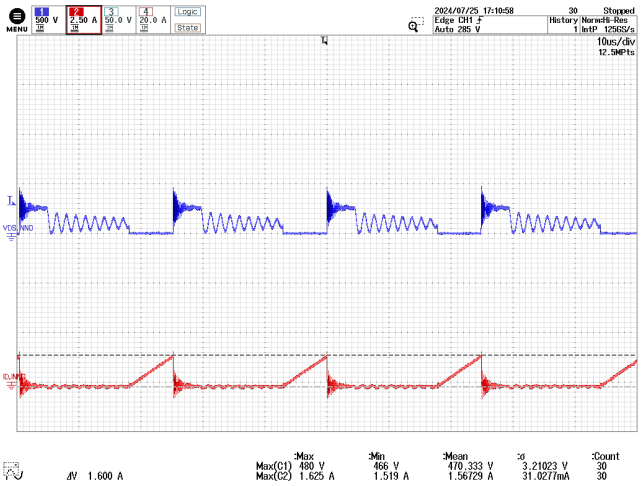


Figure 165 – INN3949FQ Drain Voltage and Current.
100 VDC, 1.5 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

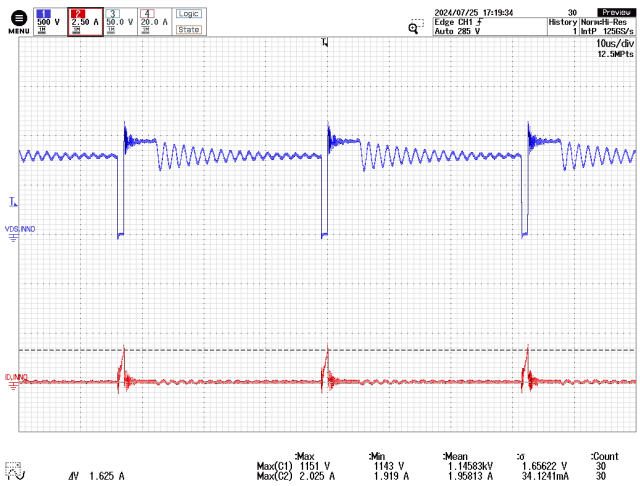


Figure 166 – INN3949FQ Drain Voltage and Current.
800 VDC, 1.5 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

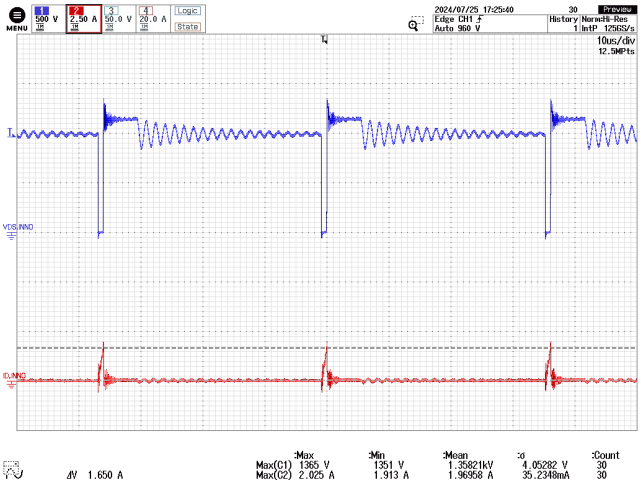


Figure 167 – INN3949FQ Drain Voltage and Current.
1000 VDC, 1.5 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

12.2.3.1.2 SR FET Drain Voltage and Current at -40 °C Ambient

Figure 168 – SR FET Drain Voltage and Current.
100 VDC, 1.5 A Load, -40 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

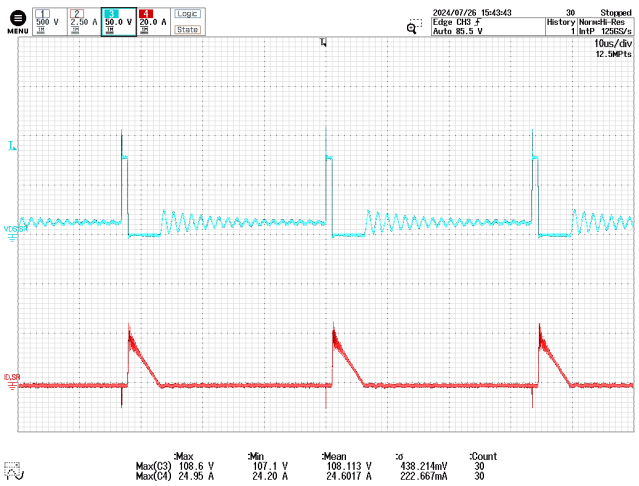


Figure 169 – SR FET Drain Voltage and Current.
800 VDC, 1.5 A Load, -40 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

Figure 170 – SR FET Drain Voltage and Current.
1000 VDC, 1.5 A Load, -40 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

12.2.3.2 Normal Operation Component Stresses at 36 W Continuous Output [45,46]

Steady-State Switching Waveforms -40 °C Ambient, 3 A, 36 W Peak Output Power						
Input	**INN3949FQ**			**SR FET**		
V_{IN} (VDC)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**
100	1.78	528	31.1	26.3	24	16.0
800	1.88	1210	71.2	28.4	108	72.0
1000	1.90	1420	83.5	29.5	128	85.3

Table 17 – Summary of Voltage Stress on Critical Components at -40 °C Ambient, 3 A Load, 36 W Peak Output Power.

[45] SR FET current is the sum of Q1 and Q2 currents.
[46] SR FET voltage was taken from Q1.

12.2.3.2.1 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient

Figure 171 – INN3949FQ Drain Voltage and Current.
100 VDC, 3 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

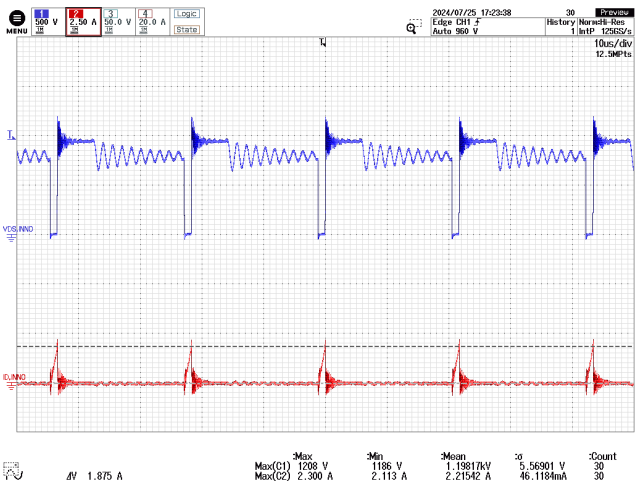


Figure 172 – INN3949FQ Drain Voltage and Current.
800 VDC, 3 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

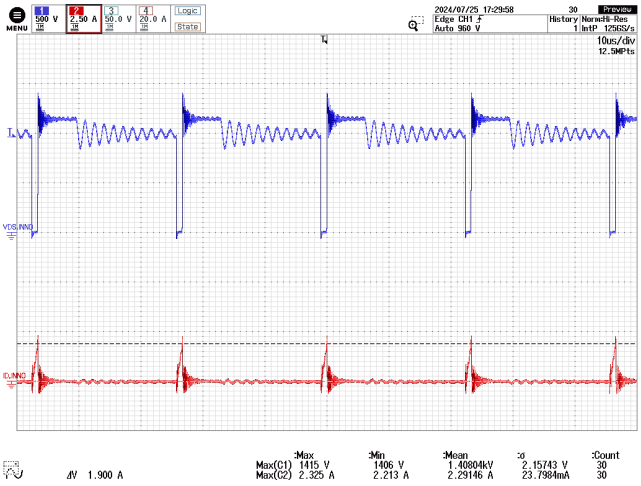


Figure 173 – INN3949FQ Drain Voltage and Current.
1000 VDC, 3 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

12.2.3.2.2 SR FET Drain Voltage and Current at -40 °C Ambient

Figure 174 – SR FET Drain Voltage and Current.
100 VDC, 3 A Load, -40 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

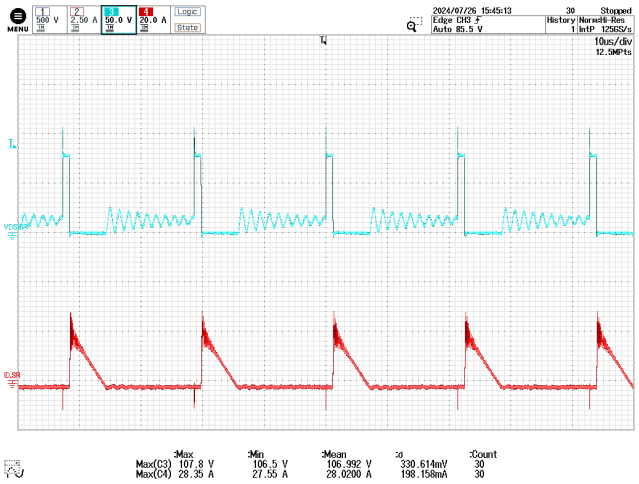


Figure 175 – SR FET Drain Voltage and Current.
800 VDC, 3 A Load, -40 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

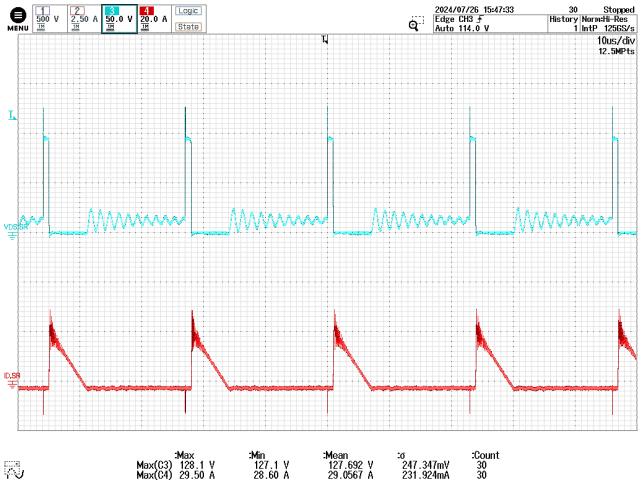


Figure 176 – SR FET Drain Voltage and Current.
1000 VDC, 3 A Load, -40 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

12.2.3.3 Normal Operation Component Stresses at 24 W Peak Output Power[47,48]

Steady-State Switching Waveforms -40 °C Ambient, 2 A, 24 W Peak Output Power						
Input	**INN3949FQ**			**SR FET**		
V_{IN} (VDC)	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**	**I_D (A)**	**V_{DS} (V)**	**V_{STRESS} (%)**
100	1.7	496	29.2	25.3	24.8	16.5
800	1.73	1170	68.8	26.7	108	72.0
1000	1.8	1390	81.8	27.5	129	86.0

Table 18 – Summary of Voltage Stress on Critical Components at -40 °C Ambient, 24 W Peak Output Power.

[47] SR FET current is the sum of Q1 and Q2 currents.
[48] SR FET voltage was taken from Q1.

12.2.3.3.1 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient

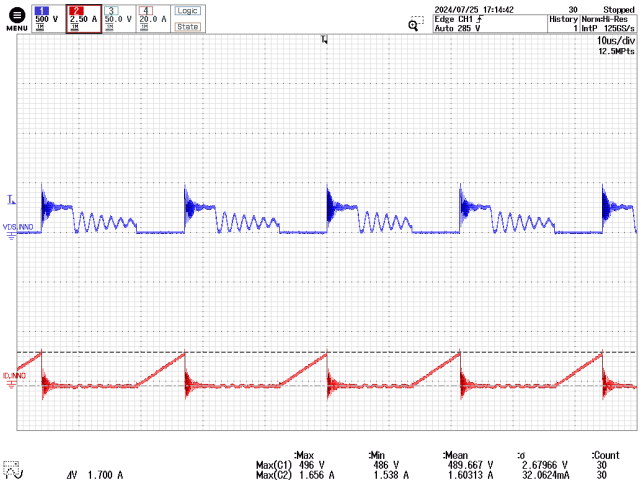


Figure 177 – INN3949FQ Drain Voltage and Current.
100 VDC, 2 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

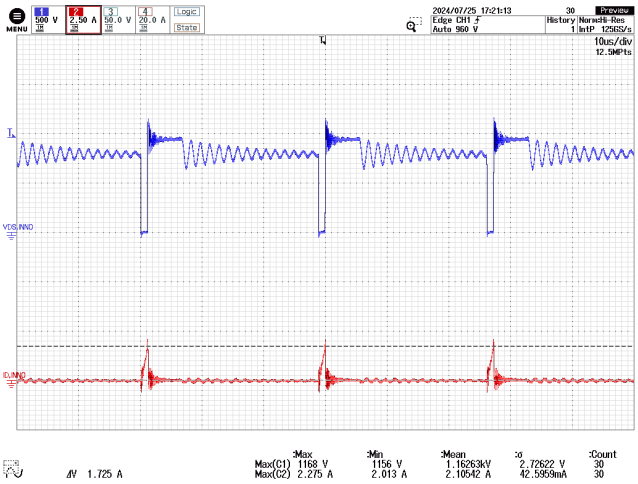


Figure 178 – INN3949FQ Drain Voltage and Current.
800 VDC, 2 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

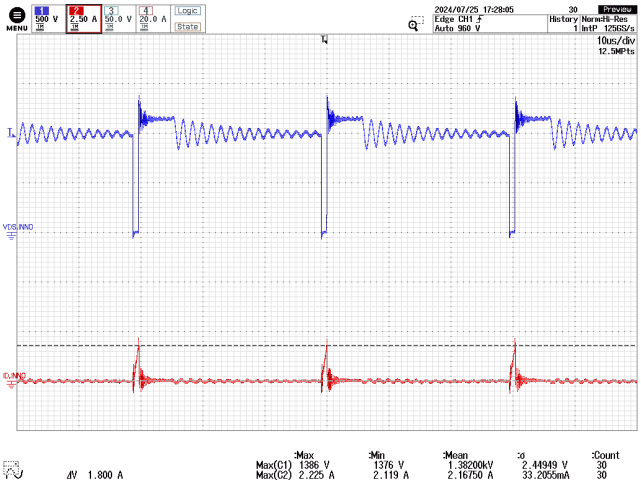


Figure 179 – INN3949FQ Drain Voltage and Current.
1000 VDC, 2 A Load, -40 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
Time: 10 µs / div.

12.2.3.3.2 SR FET Drain Voltage and Current at -40 °C Ambient

Figure 180 – SR FET Drain Voltage and Current.
100 VDC, 2 A Load, -40 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

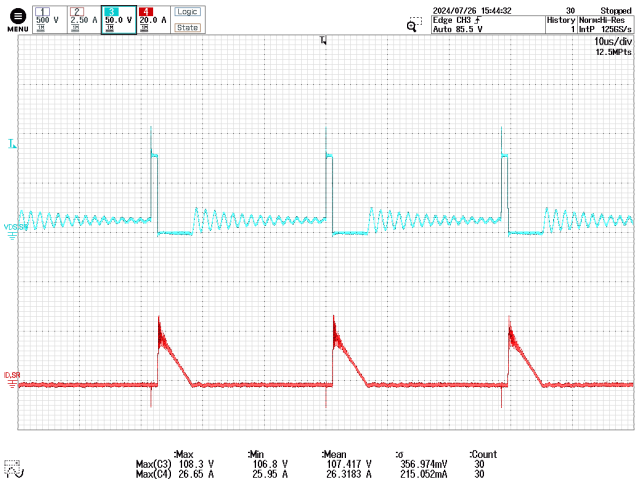


Figure 181 – SR FET Drain Voltage and Current.
800 VDC, 2 A Load, -40 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

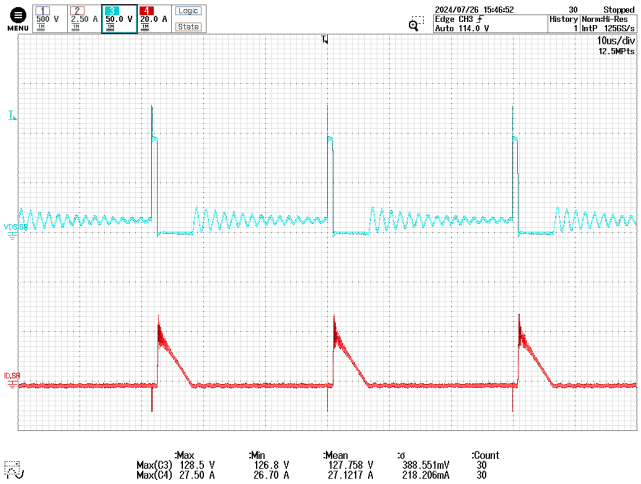


Figure 182 – SR FET Drain Voltage and Current.
1000 VDC, 2 A Load, -40 °C Ambient.
CH3: $V_{DS,SR}$, 50 V / div.
CH4: $I_{D,SR}$, 20.0 A / div.
Time: 10 μs / div.

12.3 Load Transient Response

Output voltage waveforms were captured under dynamic loading from 0% to 50%, 50% to 100%, and 10% to 90%. The time duration for the load at each state was set to 100 ms with a load slew rate of 100 mA / μs. The test was performed at 85 °C ambient.

Dynamic Load Settings	V_{IN} (VDC)	$V_{OUT(MAX)}$ (V)	$V_{OUT(MIN)}$ (V)
0% - 50% - 0% (0 A - 0.75 A – 0 A)	100	12.2	11.8
	800	12.3	11.9
	1000	12.3	11.8
50% - 100% - 50% (0.75 A - 1.5 A – 0.75 A)	100	12.1	11.9
	800	12.3	11.9
	1000	12.5	12.1
10% - 90% - 10% (0.15 A - 1.35 A – 0.15 A)	100	12.1	11.8
	800	12.3	11.8
	1000	12.3	11.8

Table 19 – Load Transient Response.

12.3.1 Output Voltage Ripple with 0% - 50% - 0% Transient Load at 85 °C Ambient

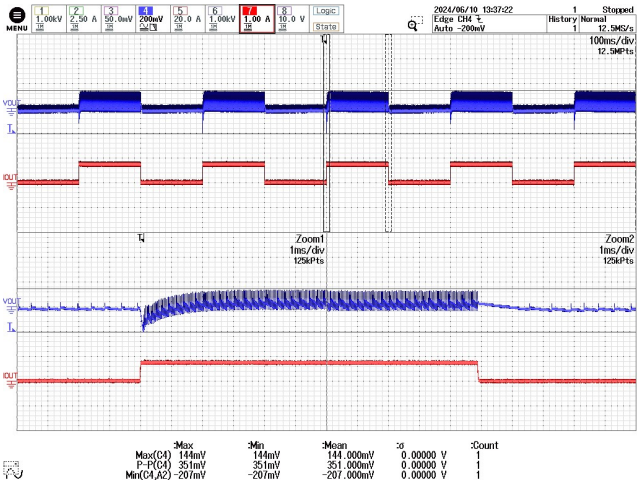


Figure 183 – Output Voltage and Current.
100 VDC, 0 A - 0.75 A - 0 A Transient Load,
85 °C Ambient.
CH4: V_{OUT}, 200 mV / div.
CH7: I_{OUT}, 1 A / div.
Time: 100 ms / div.

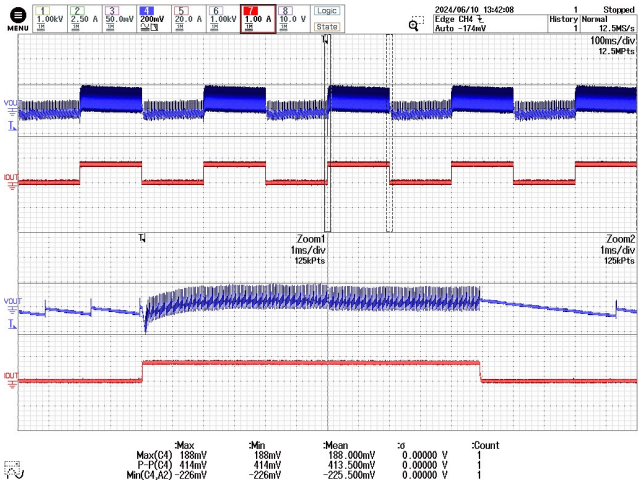


Figure 184 – Output Voltage and Current.
800 VDC, 0 A - 0.75 A - 0 A Transient Load,
85 °C Ambient.
CH4: V_{OUT}, 200 mV / div.
CH7: I_{OUT}, 1 A / div.
Time: 100 ms / div.

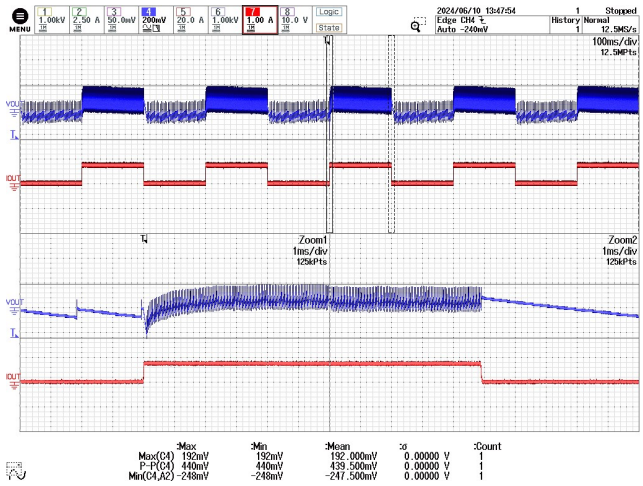


Figure 185 – Output Voltage and Current.
1000 VDC, 0 A - 0.75 A - 0 A Transient Load,
85 °C Ambient.
CH4: V_{OUT}, 200 mV / div.
CH7: I_{OUT}, 1 A / div.
Time: 100 ms / div.

12.3.2 Output Voltage Ripple with 50% - 100% - 50% Transient Load at 85 °C Ambient

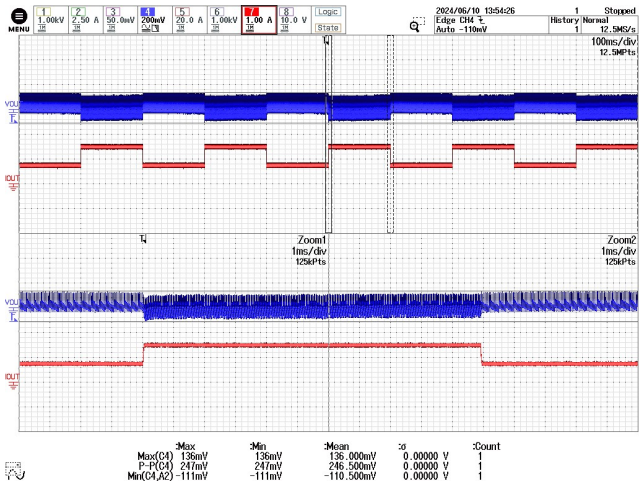


Figure 186 – Output Voltage and Current.
100 VDC, 0.75 A - 1.5 A - 0.75 A Transient Load,
85 °C Ambient.
CH4: V_{OUT}, 200 mV / div.
CH7: I_{OUT}, 1 A / div.
Time: 100 ms / div.

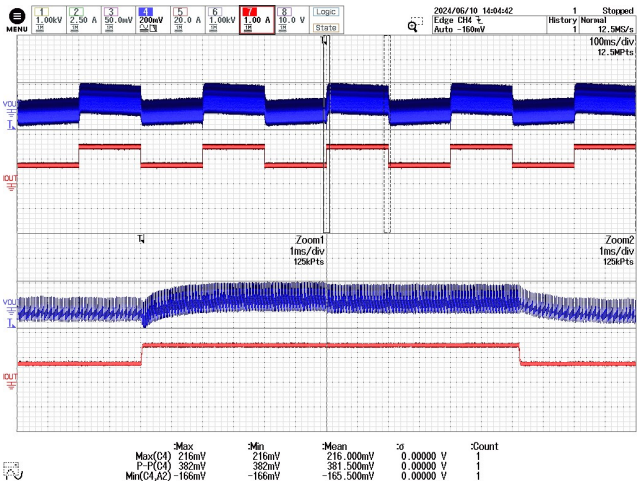


Figure 187 – Output Voltage and Current.
800 VDC, 0.75 A - 1.5 A - 0.75 A Transient Load,
85 °C Ambient.
CH4: V_{OUT}, 200 mV / div.
CH7: I_{OUT}, 1 A / div.
Time: 100 ms / div.

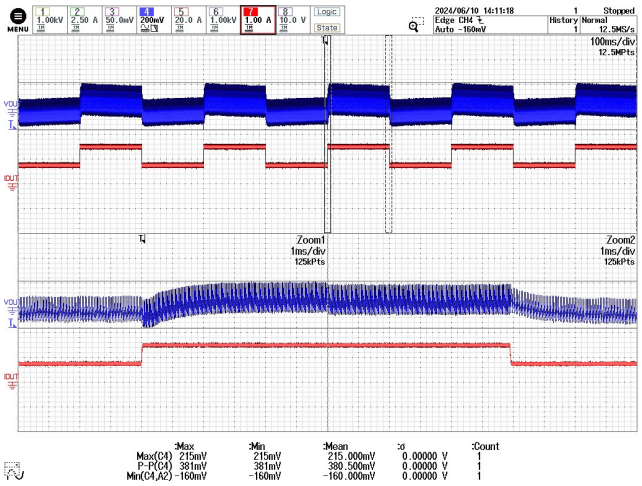


Figure 188 – Output Voltage and Current.
1000 VDC, 0.75 A - 1.5 A - 0.75 A Transient Load,
85 °C Ambient.
CH4: V_{OUT}, 200 mV / div.
CH7: I_{OUT}, 1 A / div.
Time: 100 ms / div.

12.3.3 Output Voltage Ripple with 10% - 90% - 10% Transient Load at 85 °C Ambient

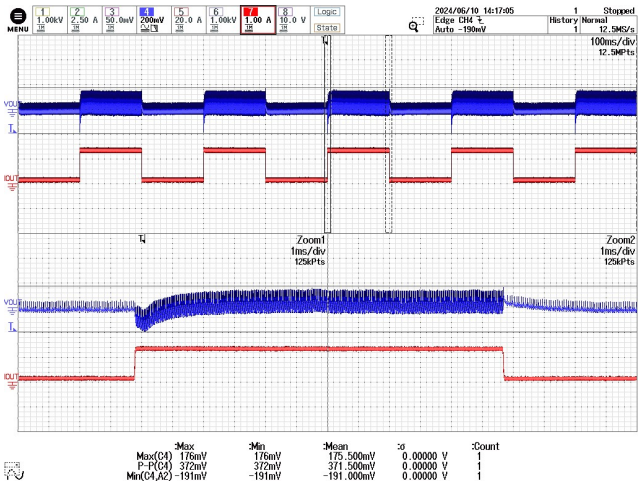


Figure 189 – Output Voltage and Current.
100 VDC, 0.15 A - 1.35 A - 0.15 A Transient Load, 85 °C Ambient.
CH4: V_{OUT}, 200 mV / div.
CH7: I_{OUT}, 1 A / div.
Time: 100 ms / div.

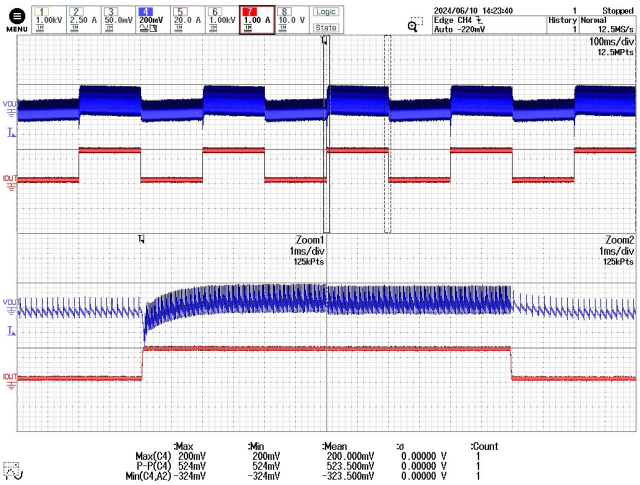


Figure 190 – Output Voltage and Current.
800 VDC, 0.15 A - 1.35 A - 0.15 A Transient Load, 85 °C Ambient.
CH4: V_{OUT}, 200 mV / div.
CH7: I_{OUT}, 1 A / div.
Time: 100 ms / div.

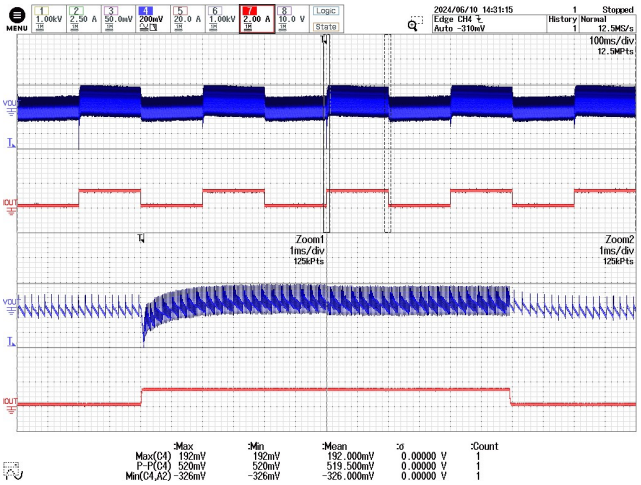


Figure 191 – Output Voltage and Current.
1000 VDC, 0.15 A - 1.35 A - 0.15 A Transient Load, 85 °C Ambient.
CH4: V_{OUT}, 200 mV / div.
CH7: I_{OUT}, 2 A / div.
Time: 100 ms / div.

12.4 Output Ripple Measurements

12.4.1 Ripple Measurement Technique

A modified oscilloscope test probe was used for output voltage ripple measurements to eliminate spurious signals due to pick-up. Figure 192 and Figure 193 below provide details of the probe modification.

A CT2708 probe adapter was affixed with a 1 μF / 50 V ceramic capacitor parallel to the probe tip and GND terminal. A twisted pair of wires kept as short as possible, were soldered directly between the probe and the output terminals.

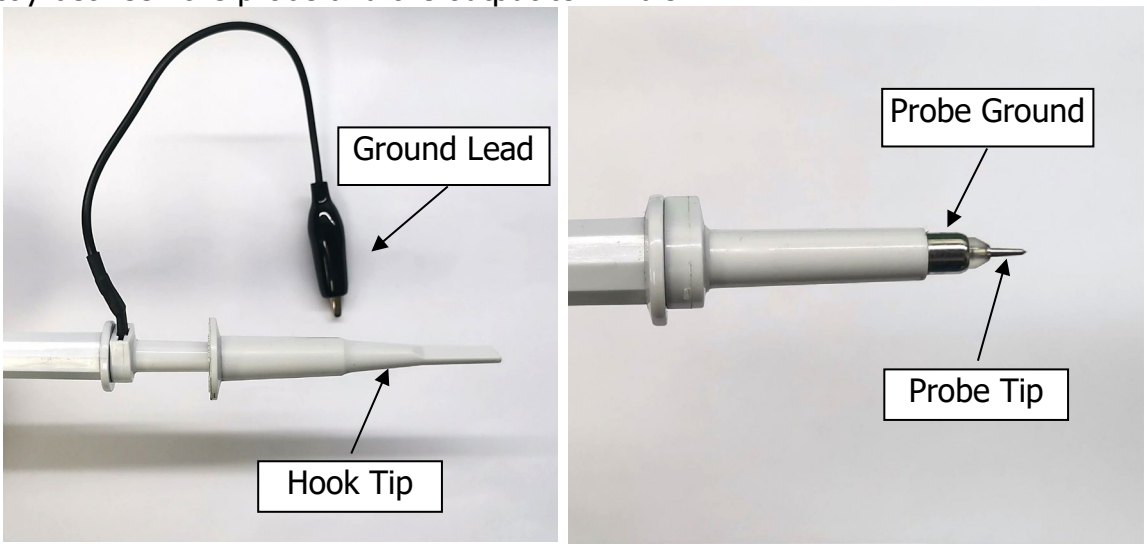


Figure 192 – Oscilloscope Probe Prepared for Ripple Measurement. (Hook Tip and Ground Lead Removed.)

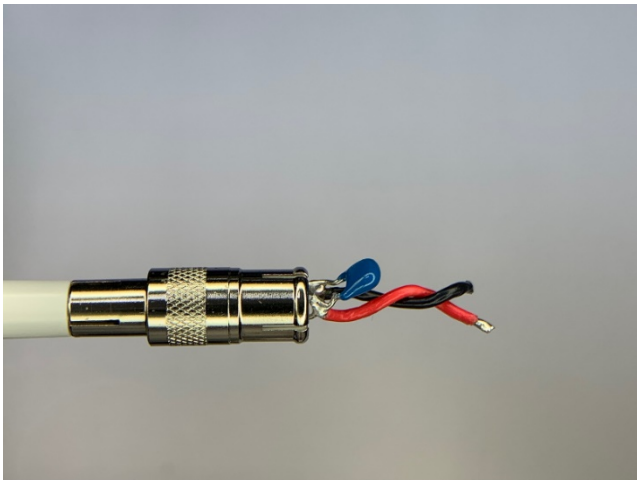


Figure 193 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurement and a Parallel Decoupling Capacitor Added.)

12.4.2 Output Voltage Ripple Waveforms

The output voltage ripple waveform was recorded at the output terminals at full load (1.5 A) using the ripple measurement probe with a decoupling capacitor.

12.4.2.1 Output Voltage Ripple at 85 °C Ambient with Constant Full Load[49]

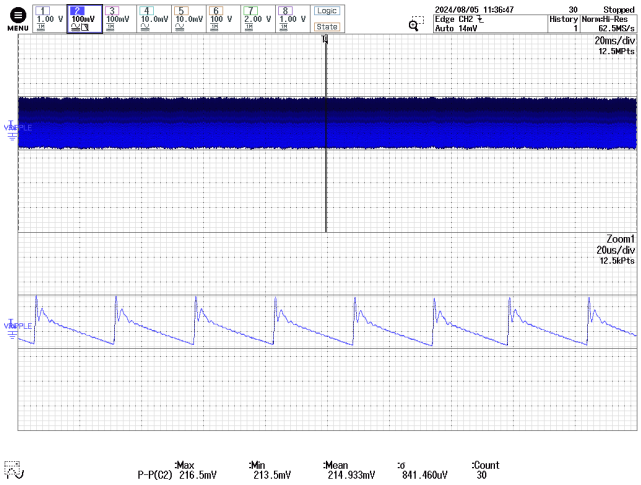


Figure 194 – Output Voltage Ripple.
100 VDC, 1.5 A Load, 85 °C Ambient.
CH2: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 215 mV.

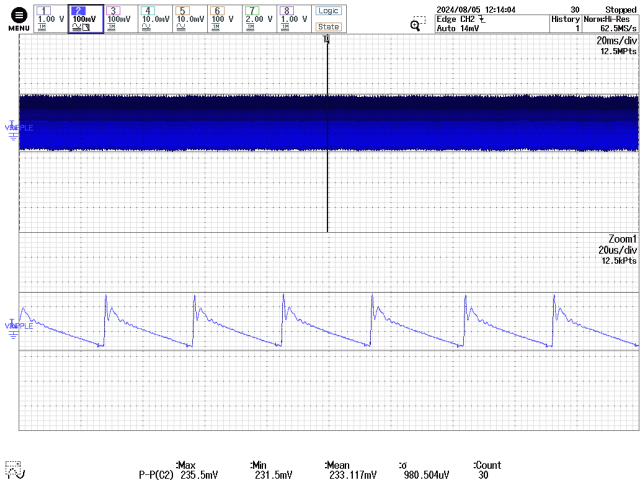


Figure 195 – Output Voltage Ripple.
400 VDC, 1.5 A Load, 85 °C Ambient.
CH2: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 233 mV.

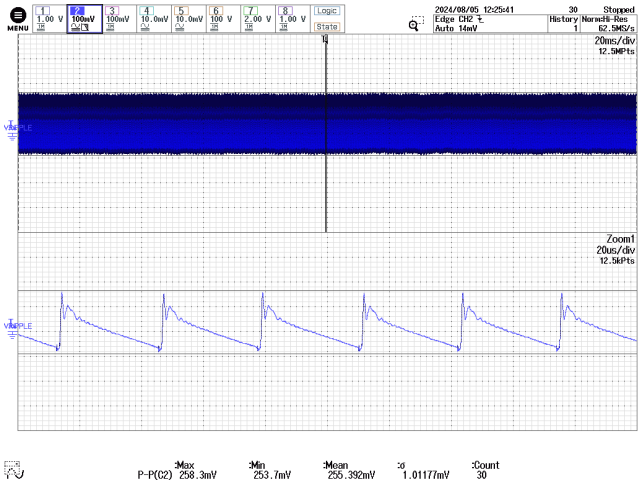


Figure 196 – Output Voltage Ripple.
800 VDC, 1.5 A Load, 85 °C Ambient.
CH2: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 255 mV.

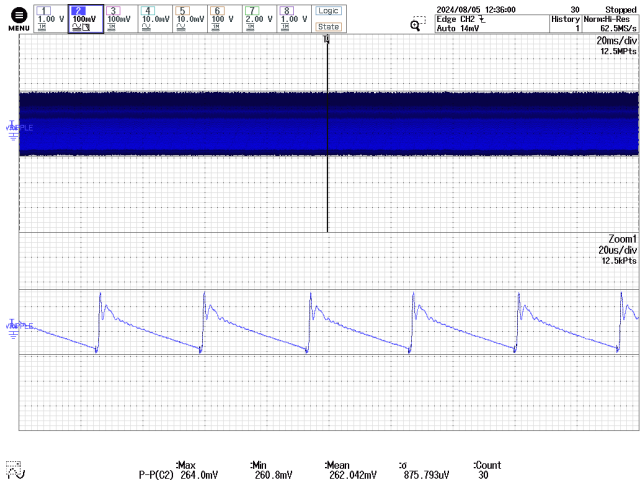


Figure 197 – Output Voltage Ripple.
1000 VDC, 1.5 A Load, 85 °C Ambient.
CH2: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 262 mV.

[49] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

12.4.2.2 Output Voltage Ripple at 25 °C Ambient with Constant Full Load[50]

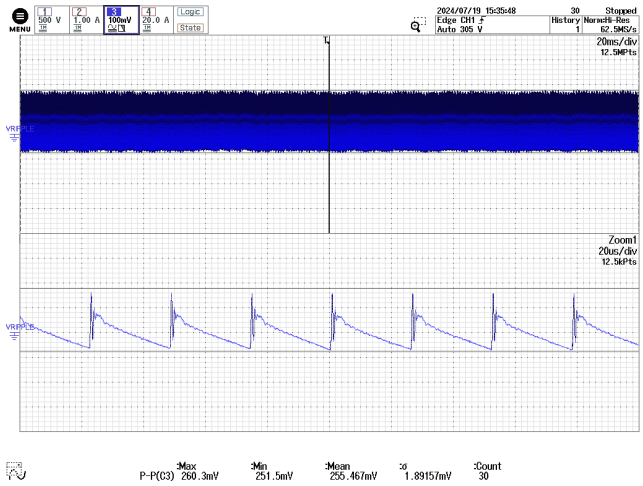


Figure 198 – Output Voltage Ripple.
100 VDC, 1.5 A Load, 25 °C Ambient.
CH3: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 255 mV.

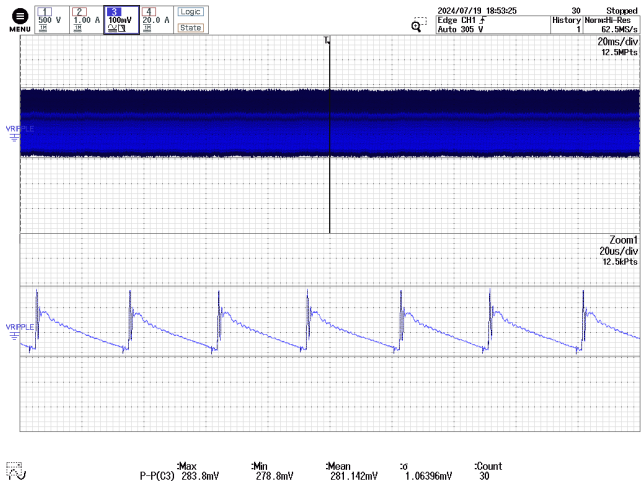


Figure 199 – Output Voltage Ripple.
400 VDC, 1.5 A Load, 25 °C Ambient.
CH3: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 281 mV.

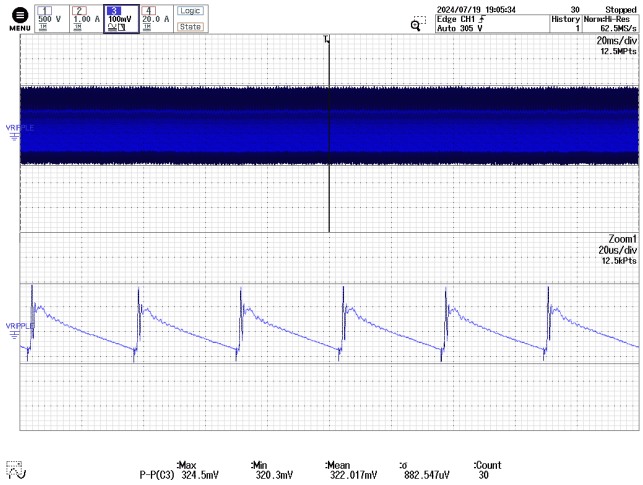


Figure 200 – Output Voltage Ripple.
800 VDC, 1.5 A Load, 25 °C Ambient.
CH3: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 322 mV.

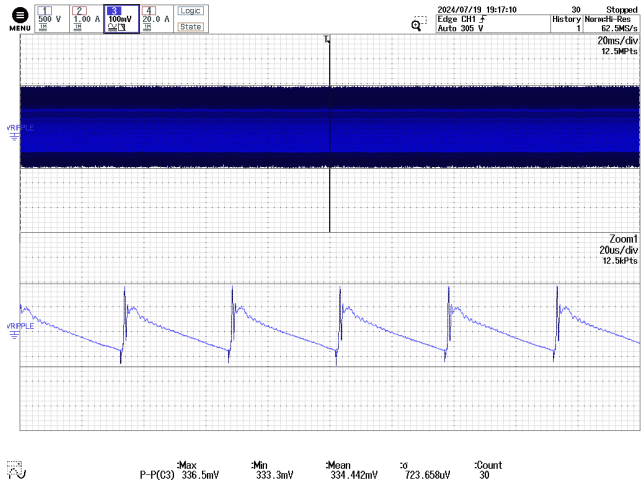


Figure 201 – Output Voltage Ripple.
1000 VDC, 1.5 A Load, 25 °C Ambient.
CH3: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 334 mV.

[50] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

12.4.2.3 Output Voltage Ripple at -40 °C Ambient with Constant Full Load[51]

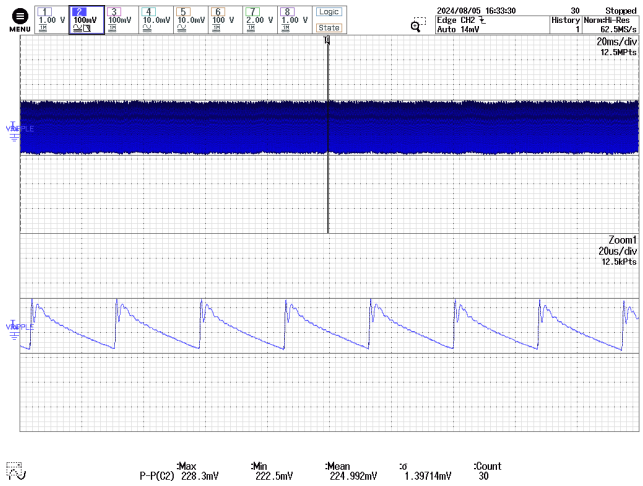


Figure 202 – Output Voltage Ripple.
100 VDC, 1.5 A Load, -40 °C Ambient.
CH2: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 225 mV.

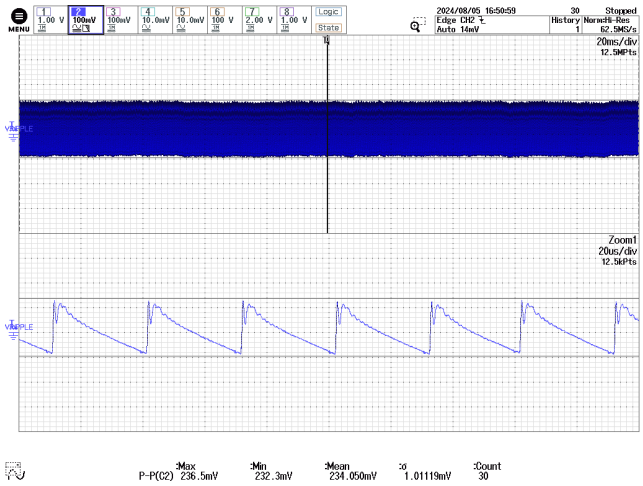


Figure 203 – Output Voltage Ripple.
400 VDC, 1.5 A Load, -40 °C Ambient.
CH2: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 234 mV.

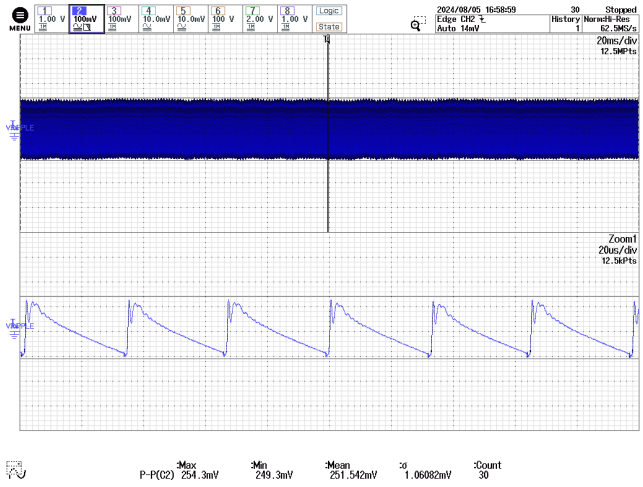


Figure 204 – Output Voltage Ripple.
800 VDC, 1.5 A Load, -40 °C Ambient.
CH2: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 252 mV.

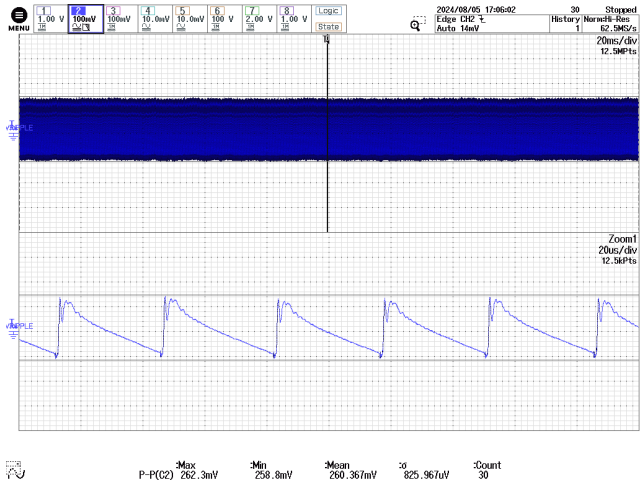


Figure 205 – Output Voltage Ripple.
1000 VDC, 1.5 A Load, -40 °C Ambient.
CH2: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 260 mV.

[51] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

12.4.3 Output Ripple vs. Load

12.4.3.1 Output Ripple at 85 °C Ambient

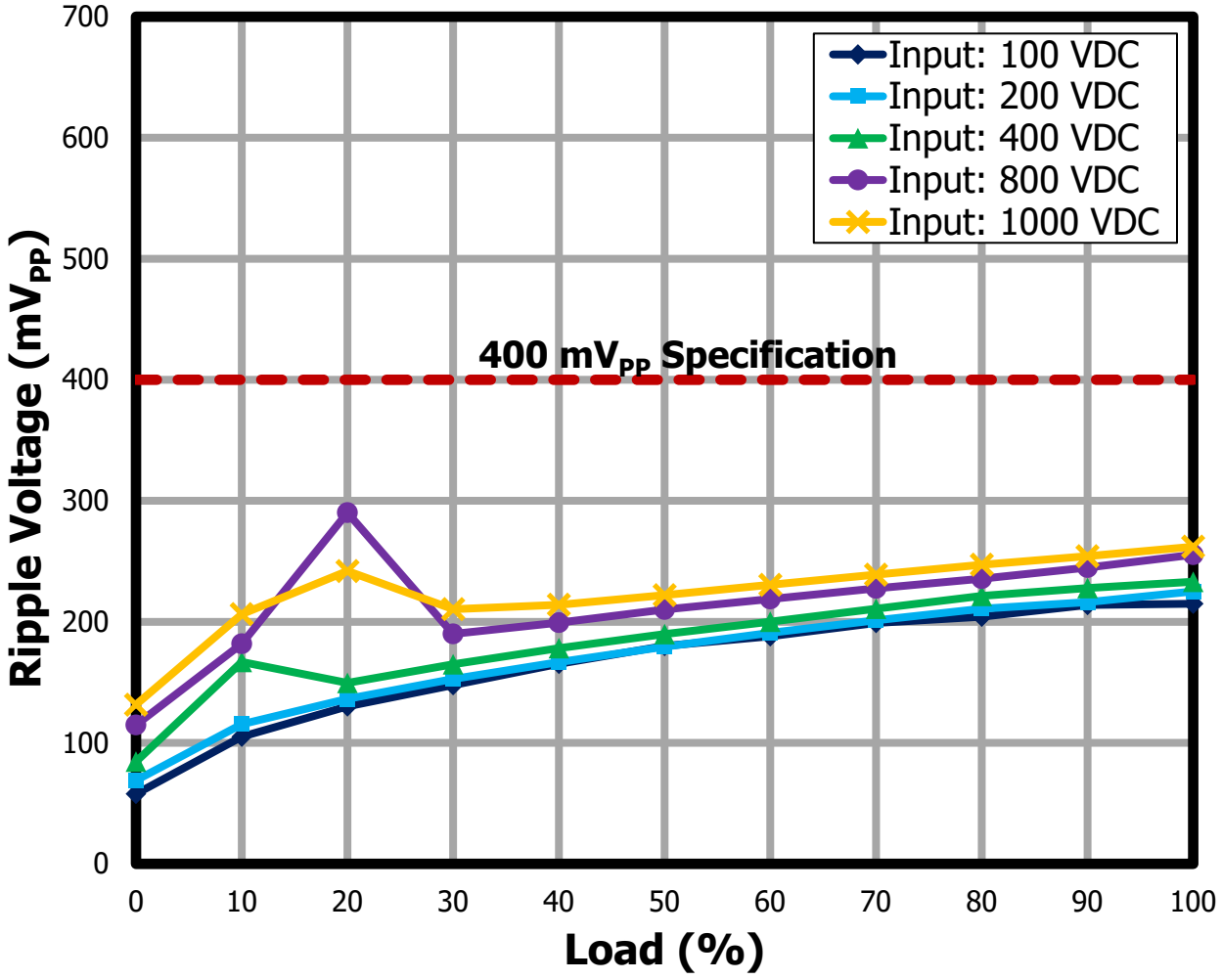


Figure 206 – Output Ripple Voltage Across Full Load (1.5 A) Range (85 °C Ambient).

12.4.3.2 Output Ripple at 25 °C Ambient

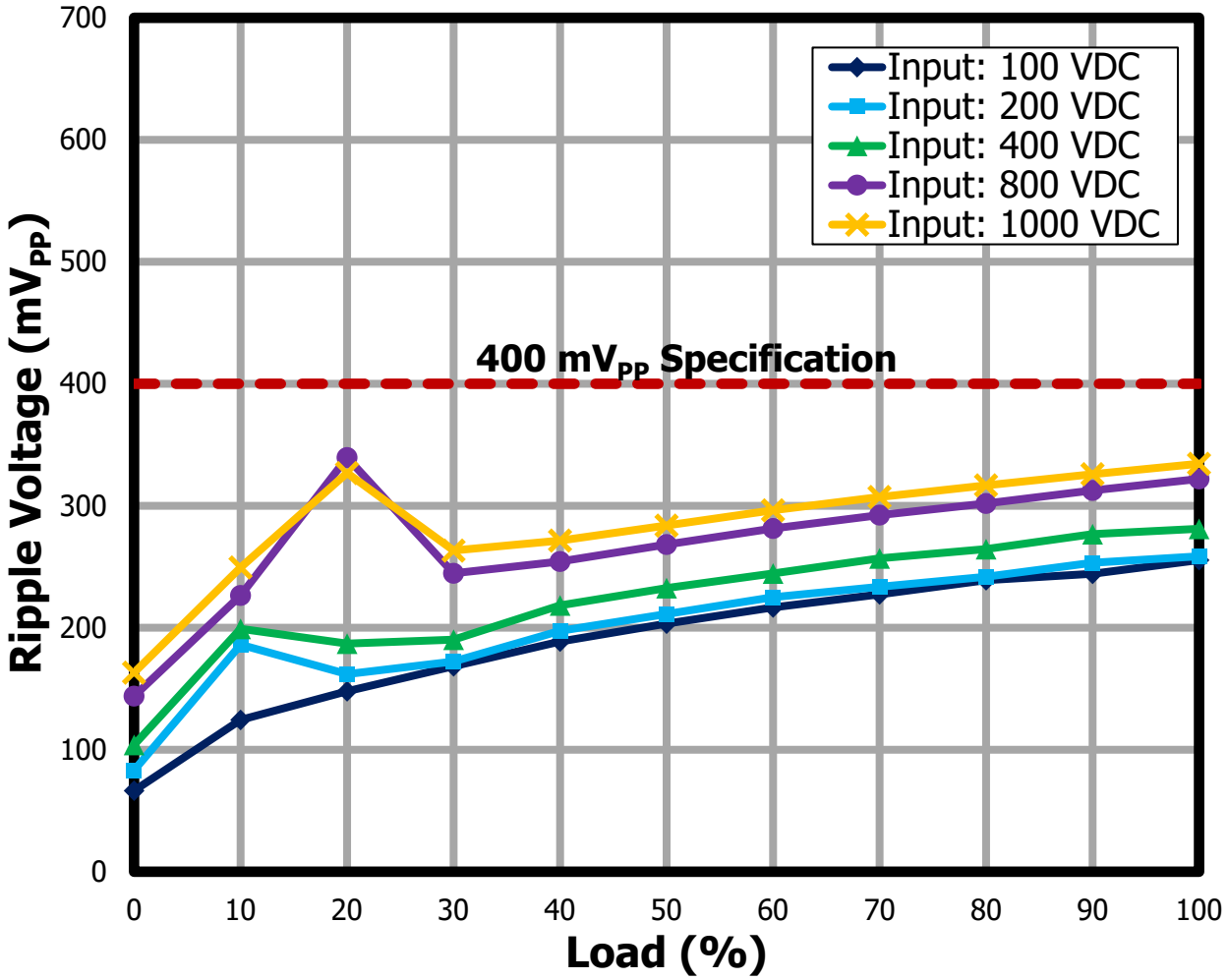


Figure 207 – Output Ripple Voltage Across Full Load (1.5 A) Range (25 °C Ambient).

12.4.3.3 Output Ripple at -40 °C Ambient

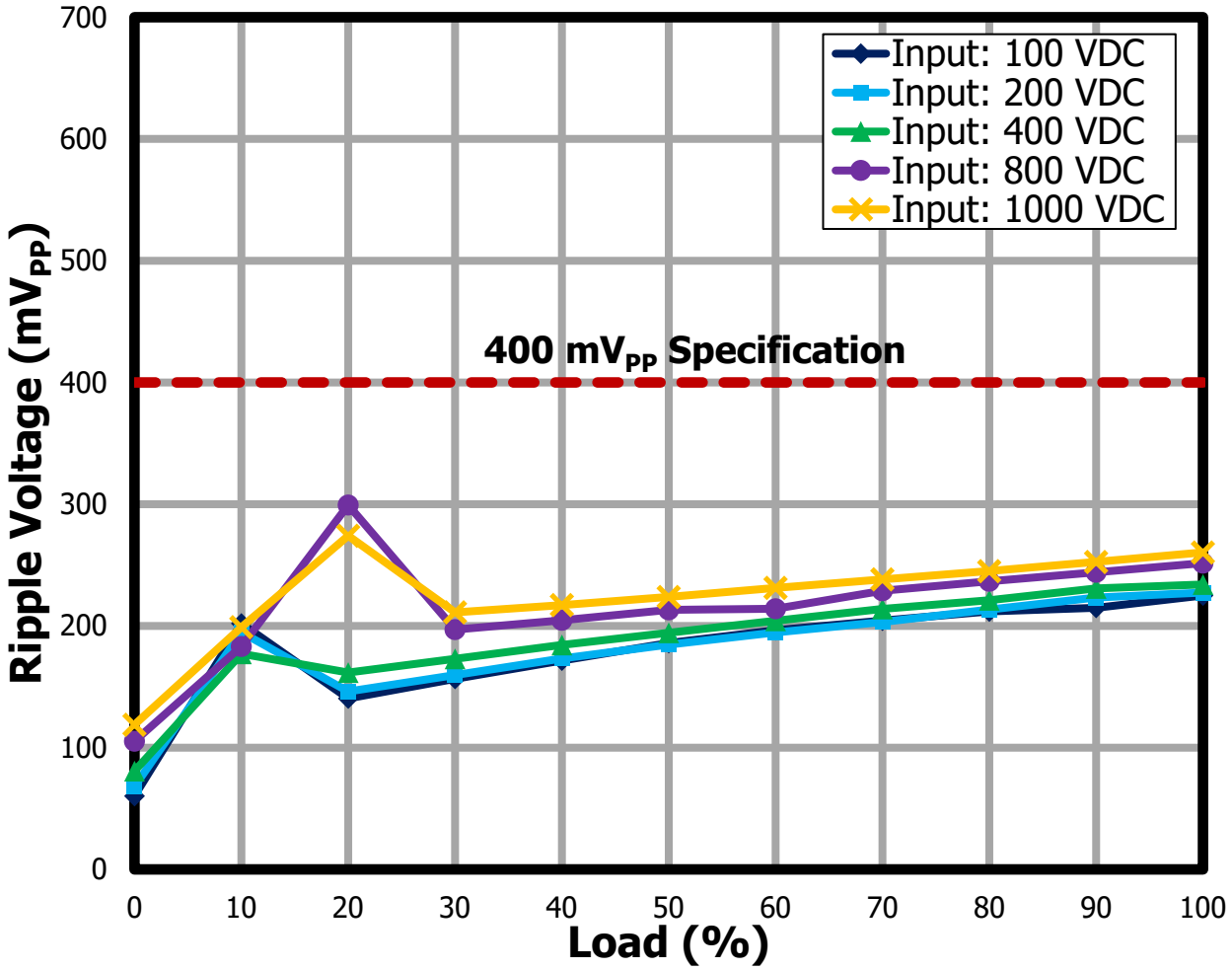


Figure 208 – Output Ripple Voltage Across Full Load (1.5 A) Range (-40 °C Ambient).

13 Output Overload

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C and allowed to stabilize for 30 minutes before turning on the unit under test. The unit was also allowed to stabilize for 20 minutes after each change in input voltage. Output voltage and output current measurements were taken 30 seconds after every change in loading condition.

Since the unit was designed for 18 W continuous power, operating beyond 3 A load might trigger overtemperature protection (OTP) before output overload is reached. A 2-minute cooling time at no-load after each change in loading condition was added to the test sequence to prevent this.

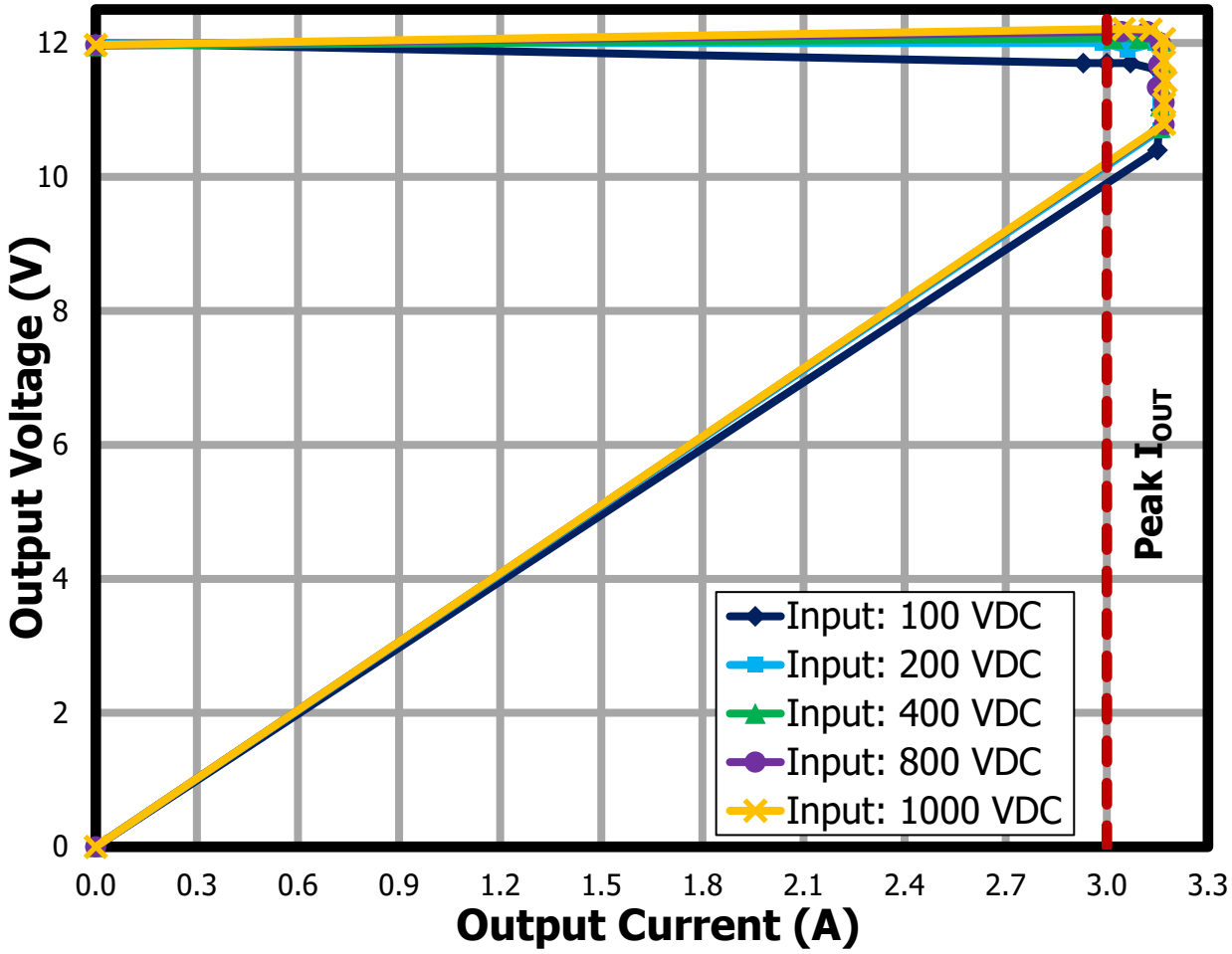


Figure 209 – Output Overload Curve at 85 °C Ambient.

14 Maximum Output Power Derating

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 105 °C and stabilized for 30 minutes before the unit under test was turned on. Maximum output power at each given input voltage was determined by finding the maximum loading condition at which the unit started up (did not enter auto-restart (AR)) or trigger any overtemperature protection. Case temperatures for critical components were also considered when determining the maximum output power capability for the power supply.

14.1 Continuous Output Power

The unit was allowed to stabilize for 30 minutes for each change in input voltage and loading condition during the start of each test sequence.

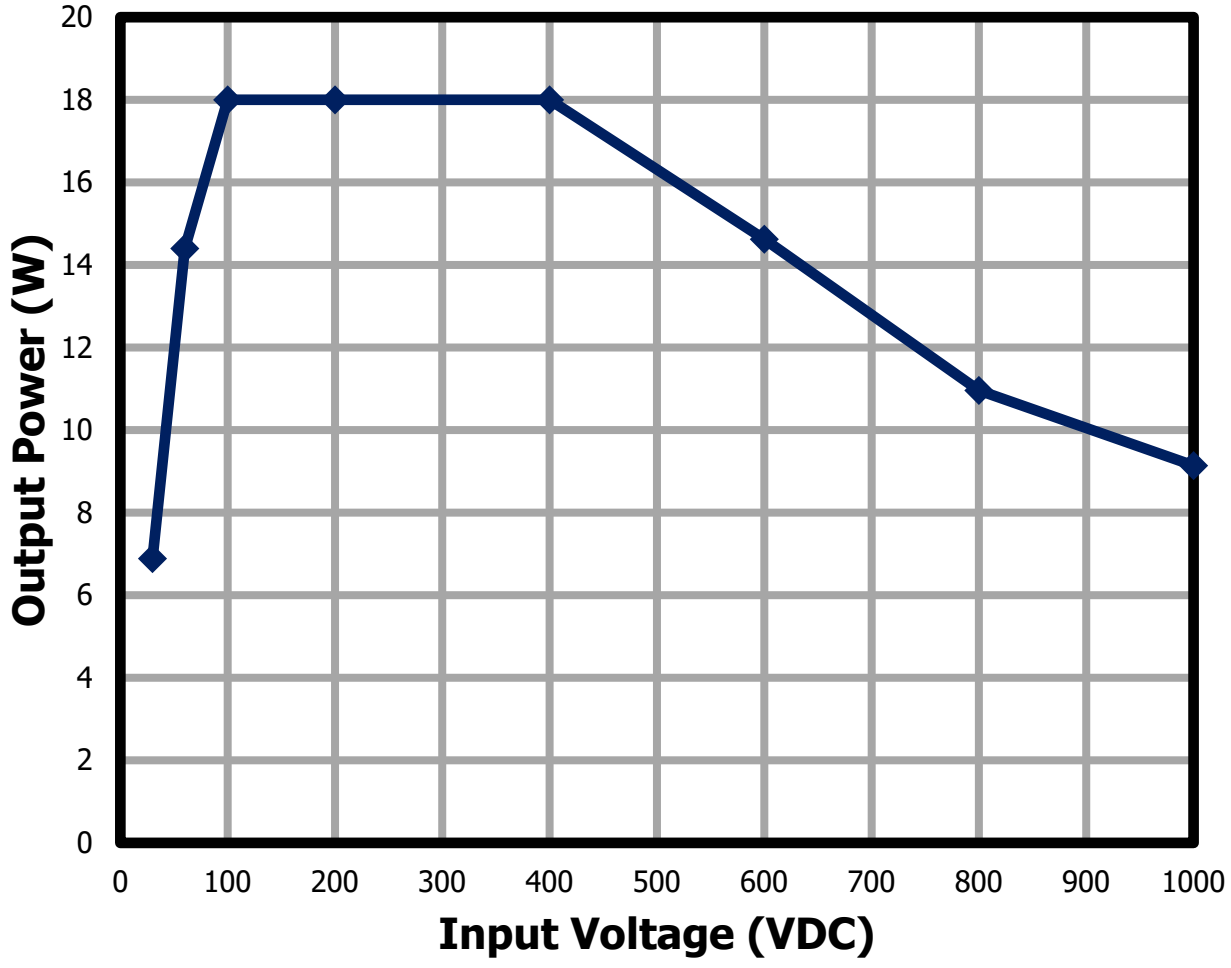


Figure 210 – Maximum Continuous Output Power Curve at 105 °C Ambient.

Input Voltage	Maximum Output Power	Limiting Factor	Value
1000 VDC	9 W	InnoSwitch3-AQ overtemperature protection	-
800 VDC	11 W	Secondary snubber resistor case temperature	> 125 °C
600 VDC	14.6 W	Secondary snubber resistor case temperature	> 125 °C
100 VDC to 400 VDC	18 W	Design maximum output power reached	-
60 VDC	14.4 W	Winding temperature	> 135 °C
30 VDC	7 W	InnoSwitch3-AQ power limit	-

Table 20 – Maximum Continuous Output Power Capability Limiting Factor at 105 °C Ambient.

14.2 Start-Up Waveform at 30 VDC Input

The measurement was taken by connecting the unit to a fully charged DC-link capacitor[52] at 30 VDC. A constant resistance load configuration was used for the start-up test.

14.2.1 Output Voltage and Current at 105 °C Ambient[53]

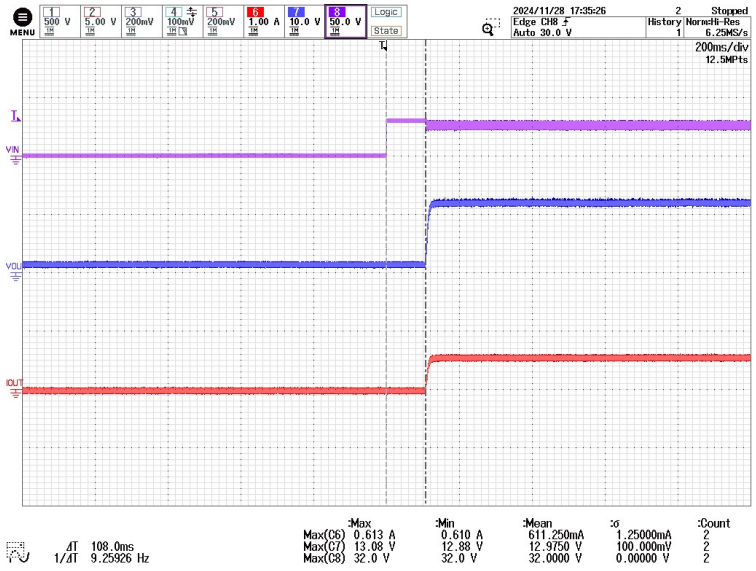


Figure 211 – Output Voltage and Current.
30 VDC, 20.6 Ω Load.
CH6: I_{OUT}, 1 A / div.
CH7: V_{OUT}, 10 V / div.
CH8: V_{IN}, 50 V / div.
Time: 200 ms / div.

[52] Inrush current was limited by adding a 10 Ω series resistor between the DC-link capacitor and the unit under test.
[53] Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.

14.3 Peak Output Power

The unit was allowed to stabilize for 30 minutes at 1000 VDC with no load before applying peak output current during the start of each test sequence.

Maximum Peak Output Power	Limiting Factor	Value
18 W for 1 Minute	InnoSwitch3-AQ overtemperature protection	-
12 W for 5 Minutes	InnoSwitch3-AQ overtemperature protection	-

Table 21 – Maximum Peak Output Power Capability Limiting Factor, 1000 VDC Input at 105 °C Ambient.

15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
14-Jan-25	NU	A	Initial Release.	Apps & Mktg

For the latest updates, visit our website: www.power.com

Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

GERMANY (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail:
singaporesales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

GERMANY (Gate Driver Sales)
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@
power.com

JAPAN
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail:
taiwansales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com